

Teoman Taskesen*, Devendra Pareek, David Nowak, Willi Kogler, Thomas Schnabel, Erik Ahlswede and Levent Gütay

Potential of CZTSe Solar Cells Fabricated by an Alloy-Based Processing Strategy

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Abstract: In this manuscript, we give an overview of the main insights into our growth procedure for kesterite solar cells and show the possibilities that are provided by this approach. The importance of using Cu–Sn alloy instead of elemental Sn and Cu in the precursor is shown. We discuss how the alloy approach stabilises the composition and helps guide the process along a preferred reaction pathway. A summary of our previously reported findings in the context of our latest results on kesterite solar cells prepared from Cu–Sn alloyed precursors is drawn. The positive impact of an alloy precursor configuration on the formation pathway, process control, and process resilience is demonstrated. Furthermore, a new optimisation strategy for kesterite, based on the reported pathway, is discussed, including a smooth phase transition from Cu-rich to Cu-poor kesterite. Finally, we demonstrate results on buffer optimisation and the application of a promising hybrid buffer configuration of CdS/Zn(O,S), which can reduce the optical losses in the solar cell structure.

Keywords: Alloy; Fabrication; Kesterite; Phase Transition; Solar Cell.

1 Introduction

In the past decades, thin-film solar cells have drawn significant attention for sustainable energy production, offering

significantly reduced raw material consumption and easy integration into applications for daily life due to their light weight and high flexibility. To date, researchers have developed several absorber materials that can be used for this technology. Among them, Cu(In,Ga)Se₂ (CIGS) is a good example that has succeeded to be commercialised and recently reached the record efficiency of 23.35 %, which is rather close to record numbers of the well-developed conventional silicon technology based on non-flexible wafer material [1]. However, CIGS suffers from the usage of expensive indium and gallium in the production. As an alternative for CIGS, the closely similar compound kesterite, Cu₂ZnSn(S,Se)₄, highlights itself with environment-friendly, earth-abundant, and low-toxicity constituent elements. This quaternary material is interesting for application in thin-film photovoltaic technology either for conventional single-junction devices or for next-generation multi-junction cells due to the possibility of its tunable band gap [2–4]. By simply changing the sulphur-to-selenium ratio in Cu₂ZnSn(S,Se)₄, the band gap can be tuned between 1 and 1.5 eV [5]. By partial replacement of elements Zn or Sn with Ge, Ba, or Cd, even a larger band gap of >1.5 eV is achievable, which is more suitable for the top layer in tandem solar cells [6–9]. This type of material could be integrated at relatively low production costs as a top layer to already existing high-efficiency photovoltaic devices with lower band gap, such as silicon or CIGS, enhancing their current efficiencies even further.

Besides the high potential of kesterite solar cells, there are also numerous challenges with the processing of this absorber material. Among these, one of the most prominent ones is the requirement for high fabrication temperatures to synthesise this quaternary material. While the minimum temperatures needed to start the formation of the kesterite compound are <400 °C, temperatures >500 °C are usually reported in the literature for obtaining better absorber properties [10]. The necessity of high processing temperatures can be troublesome if any volatile species are present during the growth. In particular, tin-chalcogenide (SnSe_{2–x} in case of pure selenide kesterite) phases, which are often observed to occur during kesterite formation, can easily escape from the absorber at these temperatures due to a high vapour pressure.

***Corresponding author: Teoman Taskesen**, Laboratory for Chalcogenide-Photovoltaics (LCP), Carl von Ossietzky University of Oldenburg, Campus Wechloy, Carl-von-Ossietzky-Straße 9-11, 26129 Oldenburg, Germany, E-mail: teoman.taskesen@uni-oldenburg.de, <https://orcid.org/0000-0002-5444-7356>

Devendra Pareek, David Nowak and Levent Gütay: Laboratory for Chalcogenide-Photovoltaics (LCP), Carl von Ossietzky University of Oldenburg, Campus Wechloy, Carl-von-Ossietzky-Straße 9-11, 26129 Oldenburg, Germany

Willi Kogler, Thomas Schnabel and Erik Ahlswede: Center for Solar Energy and Hydrogen Research Baden-Württemberg (ZSW), Meitnerstraße 1, 70563 Stuttgart, Germany

Evaporation of SnSe_{2-x} during the growth can cause several issues, such as changing the elemental composition (which influences the band gap, doping, defect clusters, and other properties), creating lateral inhomogeneities in the absorber, and forming deep energy states within the band gap of kesterite that cause enhanced non-radiative recombination and therefore lower the overall device performance [11, 12].

One of the proposed approaches to overcome the obstacle of Sn loss is the usage of a Cu–Sn alloy instead of elemental Sn at the precursor stage, which stabilises the process by keeping Sn bounded in the alloy structure during the major parts of the formation reaction, and by suppressing the formation of volatile SnSe_{2-x} phases. This appears to be more beneficial for a stable tuning of the absorber composition than compensating for possible Sn loss, for example by using excess Sn during the process.

In this article, we give a short overview on our results obtained from Cu–Sn alloy precursors and demonstrate how this approach impacts the resulting process. We further discuss the usage of elemental Sn as an additional Sn source during the annealing process, which gives the possibility to formulate a novel optimisation strategy for $\text{Cu}_2\text{ZnSnSe}_4$ (CZTSe) processing. This contains a transition from a Cu-rich to a Cu-poor composition during the high-temperature stage of the annealing process, which is similar to established processing routines in CIGS technology. Finally, the application of an alternative hybrid buffer combination to improve the spectral response of the devices will be discussed.

2 Experimental

The overall scheme of the process is demonstrated in Figure 1. Stacked elemental-alloyed layer (SEAL) precursors were deposited at room temperature by direct current magnetron sputtering (in a Von-Ardenne cluster tool) on Mo-coated soda–lime glass (SLG) substrates in SLG/Mo/Zn/Cu–Sn/Zn configuration.

The samples are then placed in a semi-closed graphite susceptor/box with elemental Se (Mateck, Jülich, Germany, 99.999%) and Sn-wire (Alpha Aeser, Haverhill, MA, USA, purity 99.998%) followed by an annealing in a conventional tube furnace from Carbolite (Neuhausen, Germany) (10 mbar N_2) at 530 °C (at 10 °C/min ramp) with 20 min dwelling time to obtain CZTSe absorber films (Fig. 2).

CdS (50 nm) was deposited on as-grown CZTSe films, by chemical bath deposition at 70 °C for 10 min. Radiofrequency sputtering was used to deposit 75 nm of i-ZnO and 500 nm Al:ZnO. The final solar cell areas were obtained by mechanical scribing, and resulting device characteristics were then measured under standard test conditions in a commercial AAA sun simulator from Photo Emission Tech (Moorpark, CA, USA). A Bentham PVE300 system (Reading, UK) was used to perform external quantum efficiency (EQE) measurements.

3 Results and Discussion

3.1 Usage of Cu–Sn Alloy as Precursor and Prevention of Sn Loss

As mentioned in Section 1, formation and evaporation of SnSe_{2-x} phases, which result in Sn loss during high-temperature kesterite processing, are commonly reported observations. Our process is formulated to avoid this

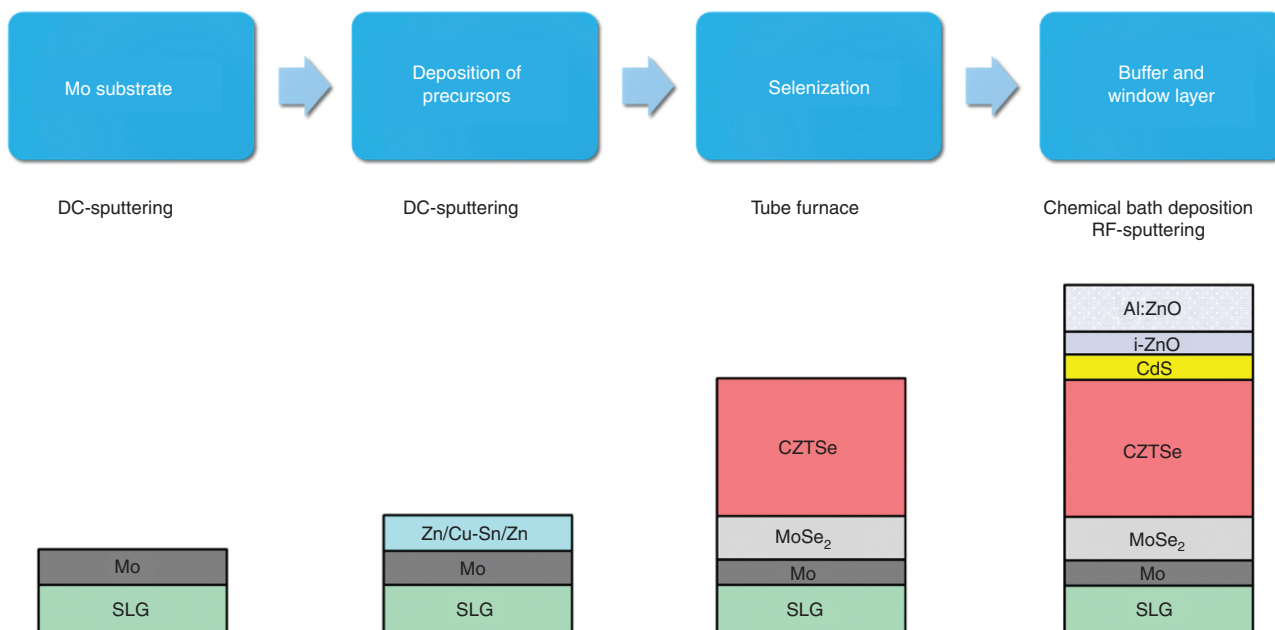


Figure 1: Fabrication scheme of CZTSe thin-film solar cells developed at the University of Oldenburg.

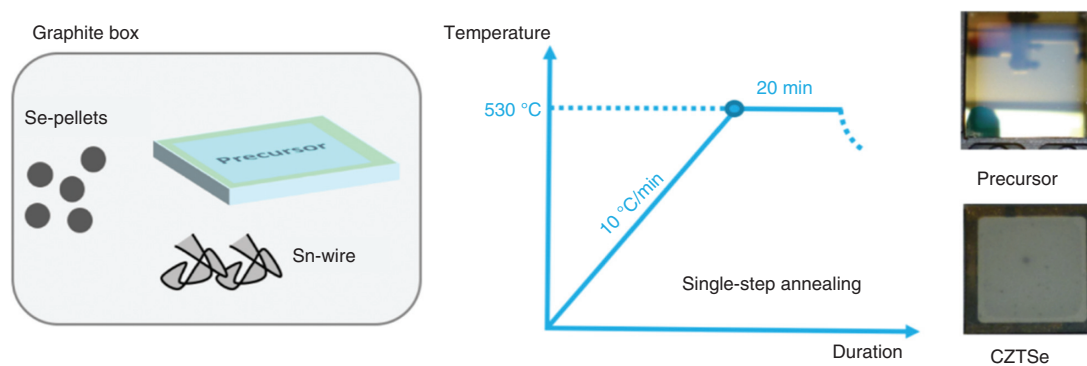


Figure 2: Precursor samples are placed inside of a graphite box with optimised amount of selenium pellets and elemental S-wire. Single-step annealing is performed. The visual changes of the sample before and after annealing are shown above.

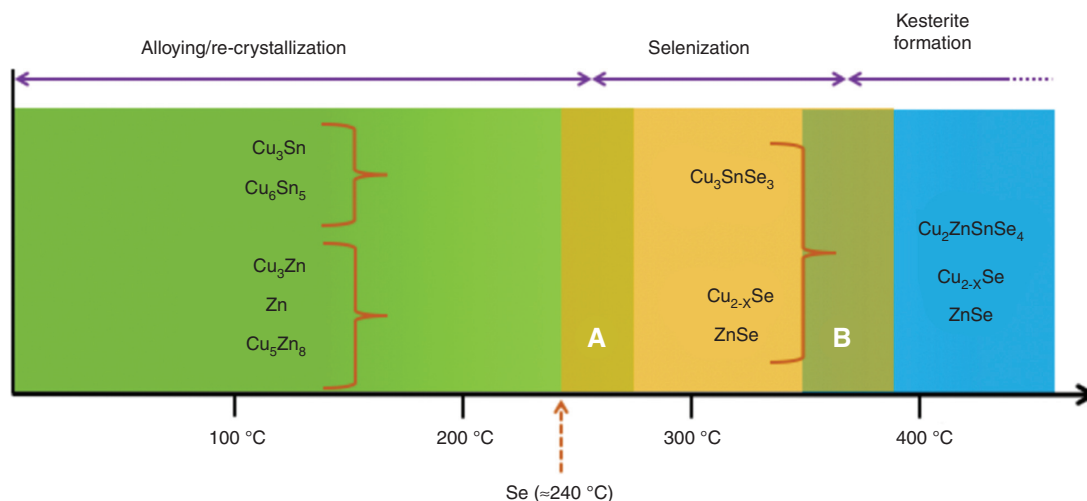
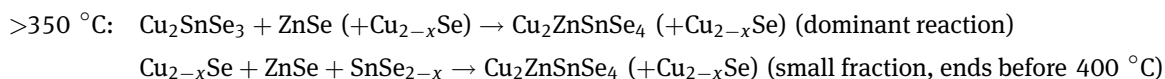
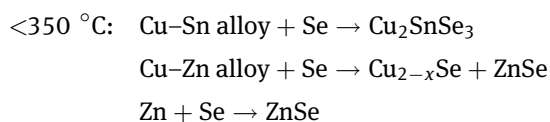


Figure 3: Summary of the initial kesterite phase formation route observed using energy dispersive X-ray diffraction and Raman measurements [13]. Zone A and zone B contain both a mix of phases from the successive stages.

problem by using a SEAL precursor. In contrast to the conventional approach of using stacked elemental precursors (Cu, Zn, Sn), the SEAL precursor contains a combination of elemental (Zn) and alloyed (Cu–Sn) layers. The usage of Cu–Sn alloy instead of elemental Sn and elemental Cu results in suppressed formation of SnSe_{2-x} , leading to kesterite formation predominantly via the reaction of alloy and/or ternary with ZnSe. These results were presented at E-MRS Spring Meeting 2019 by Gütay and will be published soon [13]. The reaction pathway is briefly summarised in Figure 3. This schematic illustrates that Sn remains in alloy form until the temperatures at which the selenium becomes active. After this temperature,

the process mainly follows the described pathway and only shows a strongly reduced formation of the SnSe_{2-x} phase, which is rapidly consumed by the process at temperatures <400 °C. This avoids the presence of volatile SnSe_{2-x} during the high-temperature annealing stage, which ultimately helps in maintaining constant Sn content in the precursor/absorber throughout the entire selenization process. Due to its minor occurrence, this path is not included in Figure 3 [13]. It must be noted that the additional Cu_{2-x}Se in brackets in the dominant reaction path represents a possible Cu excess in the initial precursor composition, which will be discussed further below.



The utilisation of Cu–Sn alloy in the precursor, however, only helps in setting a beneficial starting configuration for the process. In addition, the selenisation/annealing parameters are also crucial in order to conserve the alloy structure intact until the initiation of the selenisation reaction. The presented results by Gütay demonstrate that any un-optimised heat treatment can alter the initial phase configuration in the precursor significantly [13]. In the reported example, the altering of the initial alloy configuration resulted in the occurrence of elemental Sn, which was no longer bound to any alloy. This finding highlights that the time–temperature control during the onset of the annealing procedure is very critical and has to be optimised for keeping the previously discussed beneficial starting point intact, i.e. Sn exists only in alloyed form. Further results related to such optimum and non-optimum annealing parameters are discussed elsewhere, including the heating ramp and the base pressure in the reactor, which both determine the effective duration of heating before the onset of the selenisation reaction [14].

3.2 Phase Transition from Cu-Rich to Cu-Poor as a New Optimisation Parameter

In addition to the characteristics of the process and the basic reaction pathway discussed above, our studies further show the specific role of adding Sn-wire in the

susceptor. This elemental Sn acts as an additional tunable source of SnSe_2 during the high-temperature dwelling stage of the annealing process. However, in contrast to the common impression gained from the literature on the role of added SnSe_{2-x} or Sn during kesterite annealing, in our process the role of added Sn is not the compensation of Sn loss during the annealing. As discussed above, the stabilisation of the process by having only alloyed Sn in the precursor prevents Sn loss during kesterite growth. In our process, the main purpose of added Sn is the shifting of the overall composition of the formed kesterite towards higher Sn/Cu ratios during the very final stage of the selenisation process, which was shown to reach an increase in the range of around 30 % [13]. In the same study, we demonstrated that this inclusion of Sn at the final stage of annealing can be used for introducing a phase transition from a Cu-rich towards a Cu-poor regime during the high-temperature dwelling stage. The schematic in Figure 4 illustrates the successive stages of the process. At around 400 °C, the film contains the kesterite phase along with Cu_{2-x}Se and ZnSe, indicating a Cu-rich growth environment. At 450 °C, these phases react with SnSe_{2-x} vapour (generated due to selenisation of Sn-wire) and contributes to further growth of the kesterite phase. Incorporation of Sn to the film smoothly moves the absorber composition from the Cu-rich to the Cu-poor regime, which contains Cu-deficient single-phase CZTSe without any Cu_{2-x}Se secondary phase (similar to optimised CIGS processing, which includes an intermediate Cu-rich stage before final Cu-poor absorber composition).



Figure 4: Schematic illustration of the initial growth of Cu-rich kesterite and transition towards Cu-poor kesterite. Added elemental Sn-wire in the graphite box provides SnSe_{2-x} vapour during the high-temperature dwelling stage of the annealing and leads to Sn incorporation to the absorber.

We anticipate that the saturation of Cu vacancies during the Cu-rich stage could promote the formation of a less defective crystal structure. This could embrace less Cu vacancies, less related defect clusters, and less disorder on the Cu/Zn planes. Another beneficial effect could be an enhanced grain growth due to the recrystallisation during transition from Cu-rich to Cu-poor composition [15]. First results, which prove the practicality of this approach, have been presented by Gütay [13]. The results indicate that the starting and end points of the discussed compositional shift must be optimised independently, and can lead to further improvement of the material properties.

Such a phase transition as mentioned above opens up an entirely new parameter for optimisation. In this approach, it is possible to tune the starting and final composition independently, i.e. composition at which the kesterite crystal forms and final composition at the process termination, respectively. A schematic view of an example of such optimisation is demonstrated in Figure 5. For instance, one could start with different precursor compositions and end with the same final Cu/Sn ratio. In this case, the defect structure, existing secondary phases, film quality, and opto-electronic properties could be intentionally influenced. As known from the literature, in case of CIGS solar cells, the incorporation of a Cu-rich stage before shifting to a Cu-poor stage before process termination helped in reaching enhanced efficiencies. It has to be emphasised that the prerequisite for this type of process was the stable composition behaviour of the precursor and absorber, due to the alloy structure at the beginning of the process,

as discussed in the previous section. Only by such a stable and defined pathway can the exact tuning of the composition at the beginning of the Sn-enrichment step be possible.

3.3 Industrial Relevance of the Process

As discussed above, the Cu–Sn alloy-based precursor configuration gives the advantage of having a more stabilised formation reaction. In this section, we give an overview of the process status, which demonstrates the remarkable resilience of the process to variations of the processing parameters.

The process resilience is one of the essential points for industrial upscaling. In this context, it describes the capability of the procedure to tolerate non-optimum processing parameters while maintaining a solid efficiency for the resulting device efficiencies. In particular, for the fabrication of kesterite solar cells, variations in the amount of chalcogen availability and temperature during annealing can be crucial. In our previous work, we demonstrated that the amount of excess selenium can impact the material and opto-electronic properties of kesterite, which also influences the device performance [16]. The higher selenium amount was found to enhance the incorporation of Sn into the absorber during the high-temperature stage of the annealing via SnSe_{2-x} vapour. This leads to a slight increase in the band gap and enhances the charge carrier collection in the device, thus improving the device performance. Temperature, in a similar manner, can influence many device and thin-film properties, among other things, by changing the reaction dynamics and mobilities of compounds and elements in the solid and vapour phases, respectively. Therefore, it is essential to have a resilience to these types of parameter fluctuations. In Figure 6, the influence of combined selenium and temperature variations on device performance is presented. The selenium amount was varied from 50 mg to almost three times its value (140 mg), and temperature was changed between 510 °C and 550 °C. This range of variation can actually be considered rather large even for upscaled processes in a rough industrial environment. Therefore, the results may demonstrate the resilience to poor process control, which could lead to such extreme conditions during fabrication. Figure 6 shows that the temperature of 530 °C is at least necessary to reach device performances >9 %. The reason can be due to less Sn incorporation in case of lower chalcogen vapour pressure and an overall lower accessible amount of both Se and SnSe_{2-x} vapour in case of lower temperature. In addition, lower film quality with smaller grains and more grain boundaries is usually observed

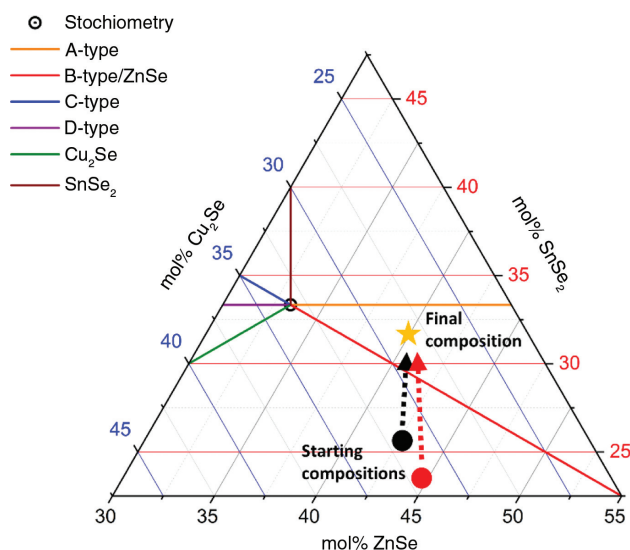


Figure 5: Scheme of an example of compositional shift during the process. The starting and final points in the phase diagram can be optimised independently for optimizing different material characteristics.

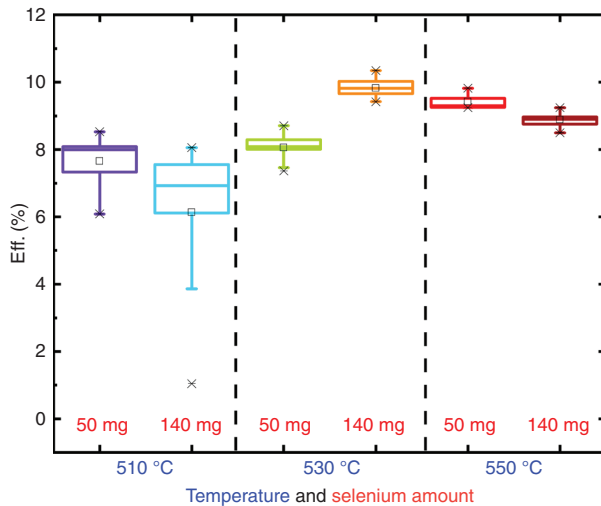


Figure 6: Influence of deviation in selenium and temperature on device performance. The process was tested for 50–140 mg between 510 °C and 550 °C.

at low temperature, which can also decrease the device performance. However, it can be seen that even at such extreme parameter variations (both temperature and selenium amount), the lowest device performance was still at the range of 7 % (for 140 mg Se at 510 °C). This underlines the resilience and stability of the process to such parameter fluctuations.

Figure 7 demonstrates the reproducibility of obtained solar cell efficiencies over the course of around 18 months. The graph contains, for the purpose of full comparability, only results of reference samples, i.e. nominally no variations of the process parameters. The documented time span covers the results obtained in the scope of a German Ministry of Education and Science–funded research project (“Free-Inca”). The first data point starts after establishing a stable process, and the time span ends with a

planned shutdown of the system for major maintenance action on the system and the laboratory infrastructure. The process shows a baseline efficiency over 9 % in a significant period of time and an average device efficiency slightly above 10 %. A similar trend can also be observed from the product of $V_{oc} \times FF$ (presented in Fig. 7b), which is less sensitive to the spectral mismatch of the sun simulator and therefore more reliable for comparisons between results obtained at different times, from different cells, and also from other research laboratories. It is also documented that during a major process breakdown due to system instabilities in the sputtering chamber during “Q4-17,” no results were obtained. In summary, it can be stated that the established processing approach as such is capable of providing a reproducible and stable baseline, which can be considered another major prerequisite for reliable application in a rough industrial context.

Another essential prerequisite for establishing a novel solar cell technology for real-life applications is the stability of fundamental device properties over an extended period of time and at effective temperatures significantly above standard test conditions. For this purpose, we investigated the long-term stability of a standard CZTSe solar cell, which is presented in Figure 8. The device had an initial efficiency of 10.6 % and was first re-measured after being stored mainly under N_2 at room temperature for >2 months. The efficiency showed a slight decrease over time, but maintained >10 % stability. Further, we performed air annealing at 85 °C for 200 h. The right part of Figure 8 displays the development during this heat exposure, which was interrupted several times for only re-measuring current–voltage (I – V) characteristics. The device still maintains efficiencies >10 % with almost no change, demonstrating a robust long-term stability of the

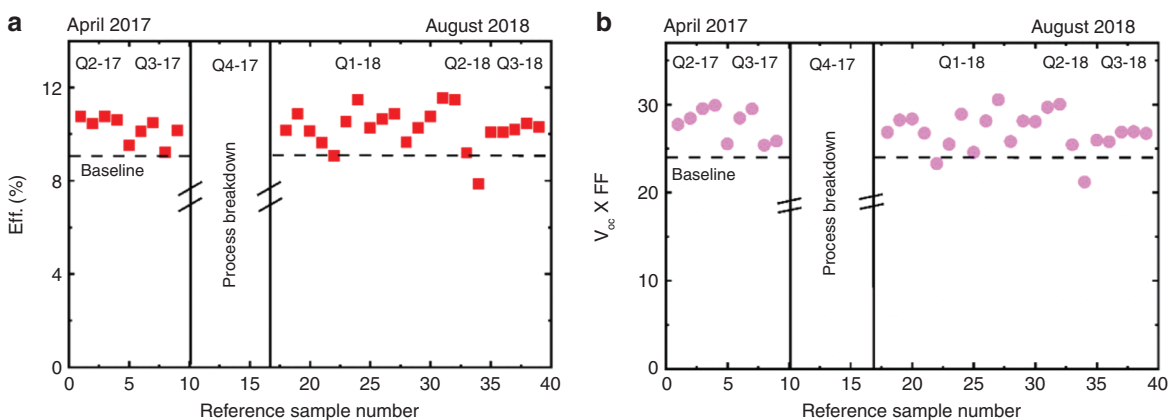


Figure 7: (a) Reference solar cell efficiencies and (b) products of $V_{oc} \times FF$ documented since reaching stable process parameters. The shown time span covers around 18 months, ending with a planned major maintenance shutdown of the system.

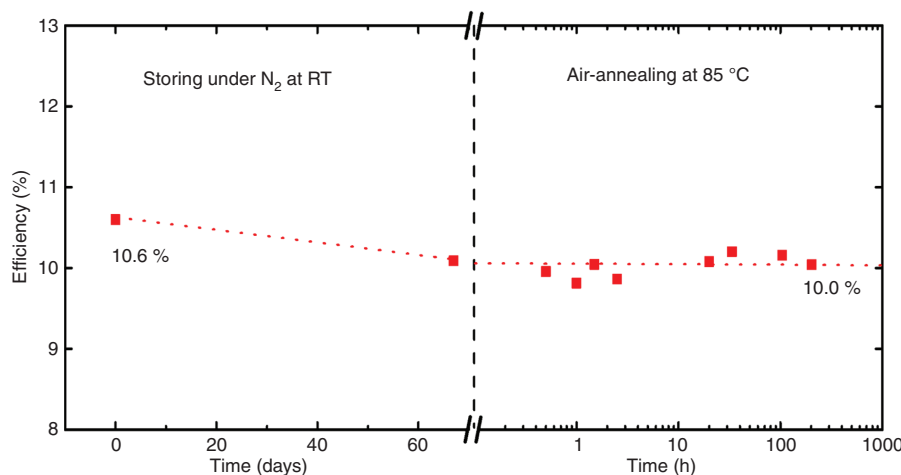


Figure 8: Impact of a long-term stability test on the efficiency of a CZTSe device. The left side of the graph shows the change of device performance after 2 months storing under N_2 atmosphere. The right side displays the impact of heat exposure at 85°C for 200 h.

CZTSe solar cells even under strong heat exposure. The reason of the slight change during the first part of the aging study is not clear yet, and according to observations on other samples the change is not necessarily always occurring in the shown decreasing direction. We also observe samples that show slightly increasing trend of efficiency over time. These differences could occur from diffusion effects at the hetero-structure interface or long-term ordering effects in the absorber, which have not been investigated yet and which can be expected to be very slow at only room temperature. It is also essential to note that the measured solar cells were not encapsulated or protected against humidity.

In Figure 9, the change in the device parameters due to low-temperature air annealing can be seen. While short-circuit current J_{sc} only fluctuates in the range of $34\text{--}35\text{ mA/cm}^2$ and does not reveal any trend over time, we can see that open-circuit voltage V_{oc} shows an increasing trend. In the literature, low-temperature annealing treatments are reported to increase the Cu/Zn ordering in the kesterite crystal, which increases its band gap. This could

be a reason for the trend observed in V_{oc} . However, fill factor FF is decreasing over time, which seems to be cancelling the positive effect of V_{oc} . The decrease of FF could be related to diffusion of elements across the interfaces, particularly between CZTSe and CdS, which could have an impact on heterojunction quality and device resistance.

3.4 Alternative Buffer Configuration

In this last section, we will touch on the topic of buffer layer optimisation, which is another possible source for further optimisation of opto-electronic properties and resulting performance of solar cell devices. From the start, the kesterite community has oriented most approaches along the known achievements of the established CIGS technology. The exact same alignment of back contact, absorber, buffer, and TCO layer, and the exact same choice of materials as in the CIGS context are still dominating. This includes the utilisation of toxic CdS as the still state-of-the-art buffer material, which is very questionable

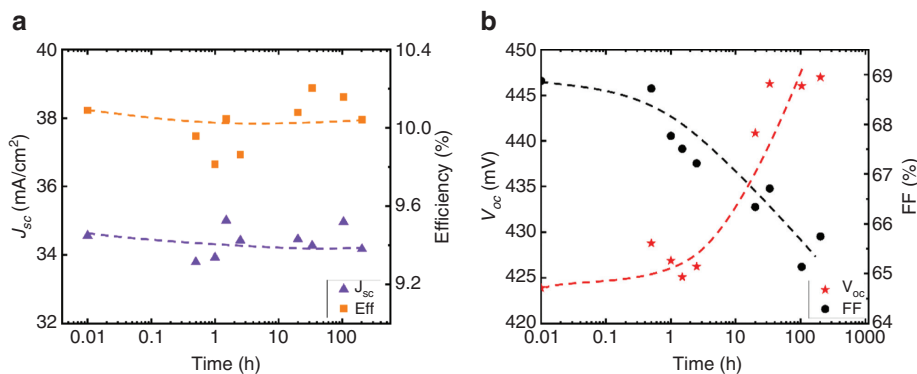


Figure 9: Influence of air annealing at 85°C for 200 h on (a) J_{sc} , Efficiency, (b) V_{oc} and FF (dashed lines are a guide to the eye).

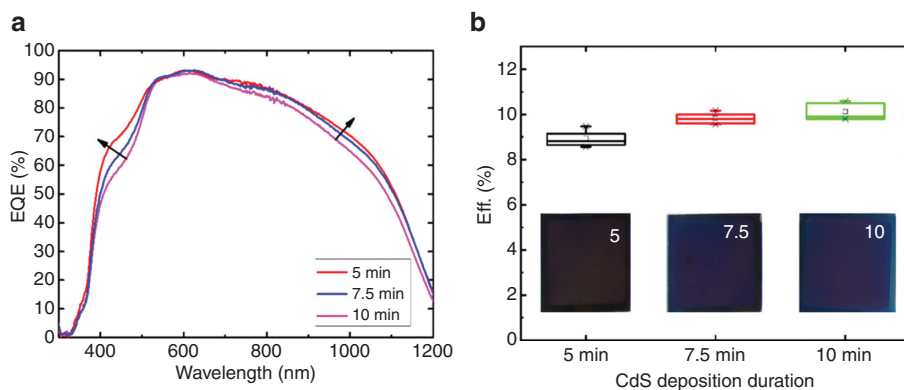


Figure 10: Influence of CdS deposition time (5, 7.5, and 10 min) (a) on EQE and (b) solar cell performance.

in the context of the otherwise sustainable and earth-abundant nature of the kesterite material family as such. However, few approaches for testing alternative back contact and buffer materials have been reported thus far in the literature, without major breakthroughs in terms of device efficiency and performance.

In the following, we show the optical losses that occur in the devices from our standard process. These losses are still dominant even in the highest-efficiency devices and lead to significant current loss at shorter wavelength [17]. This was attributed to absorption losses due to the relatively thick CdS layer, which is useful for compensating possible non-homogeneous coverage on the relatively rough CZTSe surfaces. In order to diminish these optical losses, we performed an experimental series to decrease the thickness of the CdS layer. In this series, the CdS deposition time was reduced from standard 10 min of deposition to 7.5 and 5 min in order to obtain thinner CdS layers. The EQE spectra of resulting devices are presented in Figure 10. It can be seen that decreasing the thickness of CdS clearly enhances the spectral response in the short-wavelength region with an additional slight increase at longer wavelength. The gain in the short-wavelength region is expected from less absorption in thinner CdS layers. The slightly improved situation in the long-wavelength range, however, can be related to more complex origins. Usually, this region is related to the quality of the current collection in the device. However, due to the rough surfaces that are involved here, differently thick buffer layers can also influence the light incoupling into the absorber, which can influence the effective spectral response of the device in the long-wavelength range.

However, decreasing CdS thickness does not lead to an enhancement of the device performance. The efficiency even decreases due to drop in V_{oc} and FF , indicating worse electronic behaviour of the interface for thinner buffer

layers. Therefore, simple reduction of thickness is not sufficient to obtain an enhancement in device efficiency.

A more sophisticated way for reducing the optical losses in the CdS layer appears to be the combination or replacement with a higher-band-gap buffer layer. Kogler et al. recently suggested that the hybrid buffer configuration CdS/Zn(O,S) can be a beneficial approach to enhance the spectral response and overall performance of kesterite solar cells [18].

To investigate the impact of this buffer modification on our device properties, a sample series was fabricated in collaboration with the ZSW (Stuttgart, Germany), containing devices from standard CdS, Zn(O,S), 5 nm CdS + Zn(O,S), and 30 nm CdS + Zn(O,S). Zn(O,S) layers are deposited by radiofrequency sputtering from mixed Zn(O,S) targets with the optimised composition of $[O]/([O] + [S]) = 0.8$. The solar cell results are shown in Table 1.

In agreement with the work of Kogler et al., it can be seen that a simple replacement of CdS with ZnOS leads to a dramatic efficiency drop to the range of 1 % [18]. However, the hybrid buffer combination appears to be a promising strategy for reducing optical losses and increasing solar cell performance. Figure 11 shows the measured EQE spectra of samples buffered with standard CdS (reference), 5 nm CdS + Zn(O,S), and 30 nm CdS + Zn(O,S). It can be observed that samples with Zn(O,S) and reduced CdS

Table 1: Solar cell parameters of standard CdS (reference), Zn(O,S), 5 nm CdS + Zn(O,S), and 30 nm CdS + Zn(O,S) as buffer layer.

Buffer layer	V_{oc} (mV)	FF (%)	J_{sc} (mA/cm ²)	$Eff.$ (%)
CdS	405	58	35.3	8.2
Zn(O,S)	229	23	24.0	1.3
5 nm CdS + Zn(O,S)	419	50	36.3	7.7
30 nm CdS + Zn(O,S)	437	62	36.2	9.8

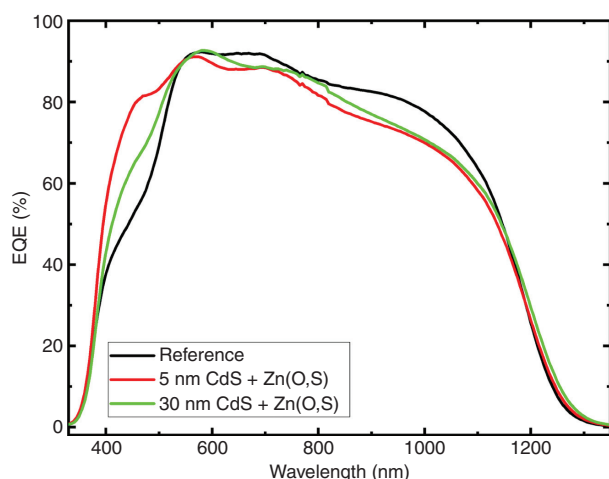


Figure 11: EQE spectra of the samples with standard CdS (reference), 5 nm CdS + Zn(O,S), and 30 nm CdS + Zn(O,S).

thickness show a significantly improved spectral response in the short-wavelength range. However, a drop is visible for longer wavelengths, which could indicate possible collection losses or altered light incoupling due to the modified optical interface, as mentioned above.

In terms of resulting efficiencies, the addition of Zn(O,S) improves most obviously the V_{oc} in the tested devices. The configuration with 30 nm of CdS interlayer between the kesterite and Zn(O,S) layers appears to be the most beneficial one, increasing device performance from 8.2 % to 9.8 % with V_{oc} improving by >30 mV. Although being only a first sample series for demonstrating the proof of applicability in our fabrication procedure, this approach is a promising step towards reducing the utilisation of toxic Cd and a possible strategy for future optimisation of optical properties and performance of kesterite solar cells.

4 Conclusion

In this manuscript, we have given a review of the main insights into our growth procedure for kesterite solar cells. We have discussed the beneficial role of using the SEAL precursor structure for guiding the process towards a preferred reaction pathway. This leads to a stabilisation of the composition in the layer and yields homogeneous spatial composition, by preventing the often reported loss of Sn during annealing of kesterites. The demonstrated process maintains solid efficiencies even for a strong variation of annealing temperature and Se amount.

We have further discussed that this approach can be used to design a new strategy for the optimisation of kesterite solar cells. The approach includes the formation of kesterite in an initially Cu-rich environment. After the

formation of kesterite, the composition is shifted to a Cu-poor environment during the high-temperature annealing stage, by supply of SnSe_{2-x} vapour. The amount of excess selenium during annealing was found to impact Sn incorporation. Having similarities with the established procedures for fabrication of high-efficiency CIGS solar cells, this approach offers new strategies for the tuning of absorber and device characteristics.

In addition, we showed an example of kesterite solar cell that remains stable for an extended time period and under high temperatures. It was shown that the efficiencies do not significantly drop and stay stable in the range of 10 %. However, the high-efficiency solar cells showed significant optical losses due to the thick CdS layer. The hybrid buffer configuration of CdS + Zn(O,S) showed promising results to overcome these types of losses in kesterite solar cells.

The combination of the reviewed findings and the added new results firmly demonstrate that kesterite solar cell technology offers aspects that make it a promising candidate for future application in the photovoltaic industry. Particularly due to its earth-abundant and less toxic constituents, it has strong benefits in terms of sustainability and environmental friendliness, and in this aspect outshines any Cd- or Pb-based technologies. However, further significant improvements of the resulting efficiencies are necessary for a leap towards the commercial utilisation of this technology.

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