

Research Article

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Coverage and reliability improvement of copper metallization layer in through hole at BGA area during load board manufacture

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Abstract: The dimple of ball grid array (BGA) area with 70 mm × 70 mm size on load board for high performance integrated circuit final test is investigated by shadow moire at first, the dimple of BGA area decreases from 184.3 to 97.1 μm when six additional prepregs with 60 mm × 60 mm size are added at BGA area before hot lamination process. The micromorphology and stress/strain simulation are conducted to improve the coverage and reliability of copper metallization layer in through hole at that BGA area. The microcracks of electroless copper layer at the position of glass fiber and inner layer copper pad, which leads to serious crack after solder float, are well covered by subsequent electroplating copper layer. When the through holes at BGA area with 0.2 mm diameter and 7.0 mm depth are fabricated based on insulating dielectric material used for high-speed signal transmission, the simulation results point out that IT968 is better than M6G for the thermal shock reliability of through hole metallization layer. A load board vehicle with 126 layers and 8.3 mm thickness based on IT968 shows good interconnection structure reliability after 12 times 288°C solder float.

Keywords: load board, through hole, simulation, metallization, microcrack

1 Introduction

With the development of 5G, artificial intelligence, augmented reality, virtual reality, big data, and high-performance computing, the demand for high-performance integrated circuit (IC) has increased significantly [1–3]. In an IC manufacture process, the final test after IC package is an essential process [4,5]. The load board is a key component that connects automatic test equipment and packaged IC [6,7]. For the manufacture of load board, the challenges include alignment among layers, fine pitch ball grid array (BGA) with through hole, drilling and metallization of high aspect ratio through hole, surface flatness, signal integrity, and so on. Furthermore, attributed to chiplet and 2.5D package technology, the chip size of high performance IC has increased to more than two reticles, the size of packaged IC has also become more and more large [8–10]. In this case, the difficulty of load board manufacture increases significantly. First, larger IC means larger BGA area on load board, the challenge of surface flatness and fine pitch BGA yield increases [11,12]. Second, high-performance IC require higher signal transmission rate, the insulating dielectric material has developed to M6G or same level material [13,14]. The new dielectric materials put forward higher requirement for seed layer coverage in through hole wall and interconnection metallization layer reliability [15–17]. Large BGA area with more through holes further increases the metallization challenge.

In general, the load board, as a specific multi-layer printed circuit board (PCB), the metallization layer in through hole includes a seed layer by electroless copper plating and a thickened layer by copper electroplating [18–21]. Compared to the normal insulating dielectric material based on epoxy, the insulating dielectric material used to load board for high-performance IC final test usually contains more inert resin for stable dielectric constant [22]. The new materials increase the risk of poor seed layer coverage. New pretreatments, such as plasma, were investigated to improve the seed layer coverage [23–27]. Besides,

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the through power of copper electroplating decreases with the increase in the aspect ratio of through hole [28–30]. As for load board, the aspect ratio of through hole increases to more than 35:1, which leads to a huge challenge to through power of copper electroplating. Usually, new formula and electroplating process development attract more research attention [19,20,29–31], but the electroless copper plating with great through power is an alternative approach to overcome this challenge [32–35]. The new challenge of electroless copper plating is how to increase the thickness of copper layer to tens of microns. Another challenge of through hole metallization layer is the reliability [36,37]. The dielectric materials used for high-speed signal transmission usually contain thermoplastic resin, such as polyphenylene oxide, which shows larger coefficient of thermal expansion of normal epoxy. In this case, the microcrack of metallization layer enhances the crack risk during reliability test [38–41]. Different insulating materials with same dielectric property also need careful evaluation of internal stress. The simulation by finite element analysis (FEA) is a widely used method for stress and strain quantification of interconnection structure of PCB [12,42–45].

In this work, the surface flatness of BGA area with 70 mm × 70 mm size is investigated by shadow moire, and additional prepregs are employed to reduce the dimple of BGA area. Then, the coverage and reliability of copper metallization layer in through hole at that BGA area is investigated by micromorphology and simulation.

2 Experimental study

2.1 Load board manufacture

Figure 1 shows a typical load board manufacture process flow.

- 1) Multiple double-side copper-clad laminates (CCLs) are baked at 193°C for 2 h. In this work, the copper foil thickness of CCL is 18, 36 or 72 μm . The insulating dielectric layer of CCL is M6G from Panasonic Corporation or IT968 from ITEQ Corporation.
- 2) Each CCL is patterned after photosensitive film attaching, exposure, developing, copper etching, and stripping.
- 3) These patterned CCLs are stacked on top of each other as designed structure, prepreg is inset between adjacent CCL. The prepreg is M6G or IT968 which is same as insulating dielectric layer of CCL. The copper foil is covered on top and bottom of the alternately stacked CCL and prepreg.
- 4) Hot lamination is done at the highest temperature higher than the glass transition temperature of prepreg.
- 5) Through holes with minimum diameter of 0.15 mm are completed by mechanical drilling.
- 6) Through hole metallization is realized by only electroless copper plating or electroplating copper on electroless copper seed layer. The minimum metallization layer thickness in through hole is 18 μm .

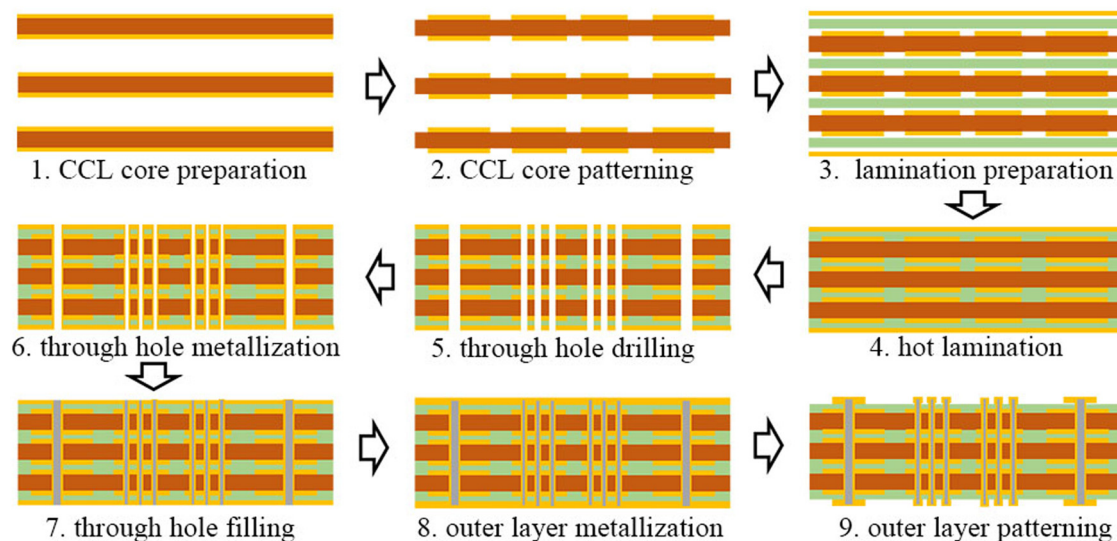


Figure 1: The schematic process flow of load board manufacture.

- 7) The through hole with metallization is filled by epoxy resin from SAN-EI KAGAKU CO., LTD. The residual resin on outer layer is cleaned by grinding.
- 8) Electroless copper plating for seed layer and electroplating copper are employed to achieve outer layer metallization.
- 9) The outer layer patterning is done in the same way as CCL patterning. Finally, the solder mask and pad treatment by electroless Ni/Au plating are finished, which is not presented in the schematic process flow.

2.2 Stress and strain simulation

The stress and strain simulation is widely used to investigate the reliability of metallization layer in through hole during heat treatment, such as reflow, thermal cycle. Usually, larger Von Mises stress and logarithm strain mean greater failure risk of metallization layer [43–45]. Figure 2 is the rectangular grid structure model of eighth through hole. Figure 2(a) is the model of through hole with copper metallization layer, while Figure 2(b) is the model of through hole with copper metallization layer after resin filling and outer layer patterning. The depth and diameter of through hole is 7.0 and 0.2 mm, respectively. The dielectric layer is M6G or IT968. The thickness of copper metallization layer in through hole is 18 μm , the diameter of pad on outer layer is 200 μm . In the condition of through hole before resin filling, the thickness of pad is 30 μm . In the condition of through hole after resin filling, the total thickness of pad is still 30 μm , the thickness of copper

covered on filling resin is 12 μm . The temperature, stress, and strain of copper metallization layer is simulated by FEA, a hexahedral mesh is used, as shown in Figure 2. An eight-node linear heat transfer brick is employed to analyze the temperature field, an eight-node linear brick with reduced integration is used to simulate the stress and strain field. The boundary conditions are set based on the true 288°C solder float for 10 s. The convective heat transfer coefficient between air and dielectric material (M6G or IT968) is 40 $\text{W}\cdot\text{m}^{-2}\cdot\text{K}^{-1}$, the convective heat transfer coefficient between air and copper layer is 80 $\text{W}\cdot\text{m}^{-2}\cdot\text{K}^{-1}$. The copper layer is bonded with dielectric material. In Figure 2(a), the top x - y plane of the model and internal surface of copper metallization layer are the heat conduction planes, while only top x - y plane of model is the heat conduction planes in Figure 2(b). The z -axis displacement of bottom x - y plane, x -axis displacement of left y - z plane, and y -axis displacement of right x - z plane are fixed. Table 1 shows the material properties at room temperature. The copper is modeled using an elasto-plastic mold, the plasticity parameter of copper is shown in Table 2, but the M6G, IT968, and filling resin are modeled as a viscoelastic material [44].

2.3 Characterization

2.3.1 BGA area dimple measurement

The dimple of BGA area is an important prerequisite for the through hole metallization. BGA area dimple increases the risk of filling resin residual on BGA area after grinding process. Filling resin residual can cause short circuit between outer layer and metallized through hole. The dimple of BGA area after hot lamination is measured by shadow moire (Akrometrix, AXP 2.0) at 25°C. Before dimple measurement, a sample with 150 mm $\times$ 160 mm size is cut from the load board, the BGA area with 70 mm $\times$ 70 mm size is located on the center of the sample.

2.3.2 Metallization layer coverage and reliability test

The metallization layer of through hole obtained from different load board process parameters is observed by optical microscope (OLYMPUS, STM6-F10-3) and scanning electron microscope (SEM) (ZEISS, Sigma 500). SEM photographs are taken at 10 kV. First, samples with less than 15 mm $\times$ 10 mm size are cut from the BGA area on load board. Next 3–12 times 288°C solder float is employed for metallization layer reliability test. Then, the sections of the sample are treated by grinding, polishing, micro etching, and so on. Finally, the metallization layer coverage and reliability are evaluated by the section image of through hole.

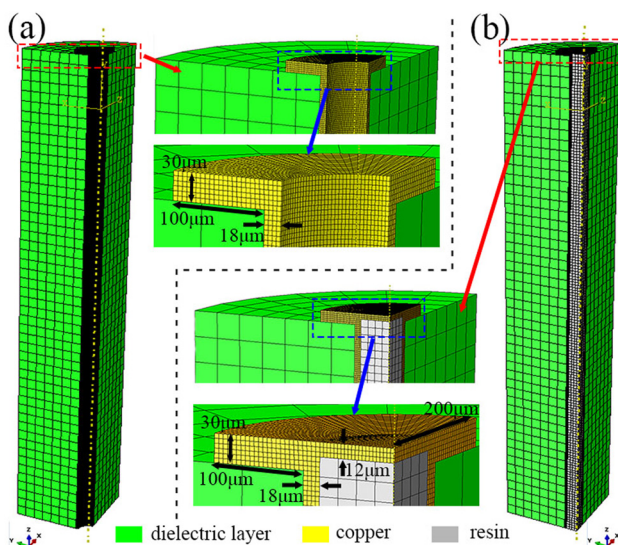


Figure 2: The rectangular grid structure model of eighth through hole. (a) Metallized through hole before resin filling and (b) metallized through hole after resin filling and outer layer patterning.

Table 1: Material properties at room temperature

Material	Unit	Copper	M6G	IT968	Filling resin
Density	$\text{kg}\cdot\text{m}^{-3}$	8,920	1,820	1,420	1,660
Thermal conductivity	$\text{W}\cdot\text{m}^{-1}\cdot\text{K}^{-1}$	400	0.42	0.54	0.54
Specific heat capacity	$\text{J}\cdot\text{kg}^{-1}\cdot\text{K}^{-1}$	390	880	1,500	1,055
Elasticity modulus	GPa	25	16.3	18	7.96
Poisson's ratio	/	0.34	0.17	0.17	0.325
Coefficient of thermal expansion (z-axis) (α_1/α_2)	$1\cdot^\circ\text{C}^{-1}$	17×10^{-6}	$60 \times 10^{-6}/360 \times 10^{-6}$	$61 \times 10^{-6}/350 \times 10^{-6}$	$39 \times 10^{-6}/105 \times 10^{-6}$

Table 2: Plasticity parameter of copper

Stress (MPa)	109	133	145	155	168	179
Strain	0	0.027	0.0367	0.055	0.093	0.129

3 Results and discussion

3.1 BGA area dimple control

Large size BGA area on load board is a significant challenge for manufacture because of greater prepreg filling requirement.

Figure 3 is a part of layout of load board. The BGA area is $70\text{ mm} \times 70\text{ mm}$, as shown in Figure 3(a). The diameter and pitch of pad on outer layer is 0.5 mm and 0.6 mm , respectively. In the interlayer, in some case, the pad position is covered by a 0.35 mm diameter copper pattern, as shown in Figure 3(b), but in other case, there is no copper pattern in pad position, as shown in Figure 3(c). The residual copper ratio in Figure 3(b) and (c) is 72.2% and 45.3% , respectively, while the average residual copper ratio of each layer is about $80 \pm 5\%$. In this case, the lower residual copper ratio in BGA area requires more prepreg during hot lamination process. In extreme case, not only the residual copper ratio of BGA area is 45.3% , but also the copper foil thickness is $72\text{ }\mu\text{m}$, leading to serious dimple at BGA area

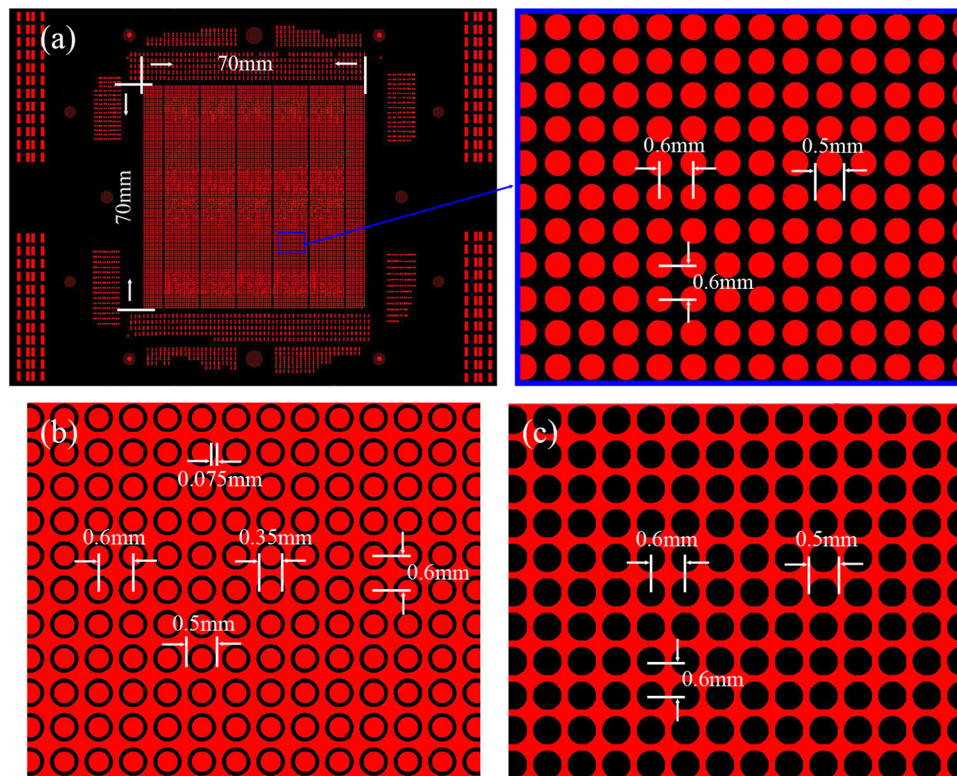


Figure 3: (a) Layout of BGA area on outer layer, (b) layout of BGA area on inner layer with high residual copper ratio, and (c) layout of BGA area on inner layer with low residual copper ratio.

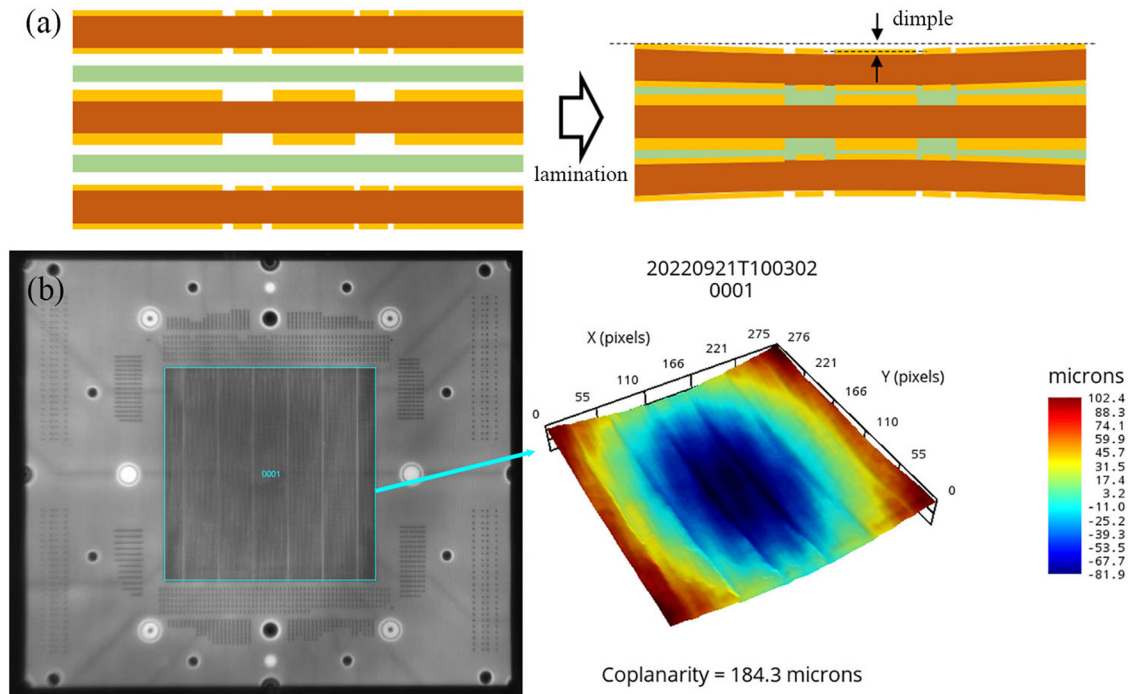


Figure 4: Dimple of BGA area on load board after hot lamination. (a) Schematic illustration of dimple formation during hot lamination and (b) dimple measurement of BGA area by shadow moire.

after hot lamination, as shown in Figure 4(a). A load board with 62 layers and 7.53 mm thickness was prepared, the dimple of BGA area is 184.3 μm which is measured by shadow moire in Figure 4(b).

To reduce the dimple of BGA area, additional prepreg is employed as shown in Figure 5. For example, if the thickness of inter layer L_m , L_n , L_{m-1} , and L_{n+1} is 72 μm , and the BGA area layout of inter layer L_m , L_n , L_{m-1} , and L_{n+1} is designed as in Figure 3(c), then an additional

prepreg is added between L_m and L_{m-1} , and between L_n and L_{n+1} . The size of additional prepreg is 60 mm $\times$ 60 mm, which is smaller than BGA area. The load board with 62 layers and 7.53 mm thickness was prepared in the condition of 2, 4, or 6 additional prepreps, Figure 6 is the dimple of BGA area which is measured by shadow moire. In this load board, there are 12 layers with 45.3% residual copper ratio BGA area which is designed as Figure 3(c), and each of these 12 layers is 72 μm thickness. It is found that the

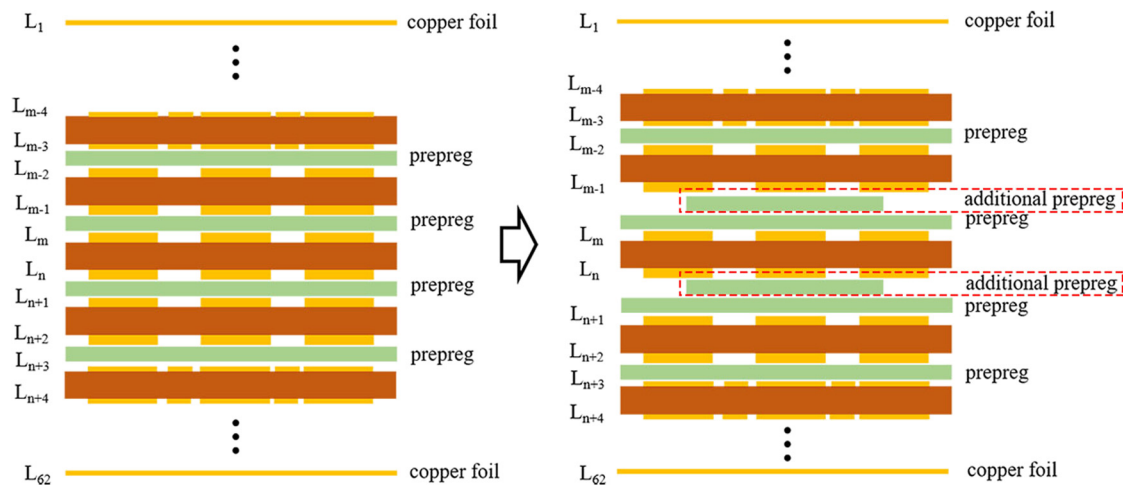


Figure 5: Schematic illustration of additional prepreg design on BGA area.

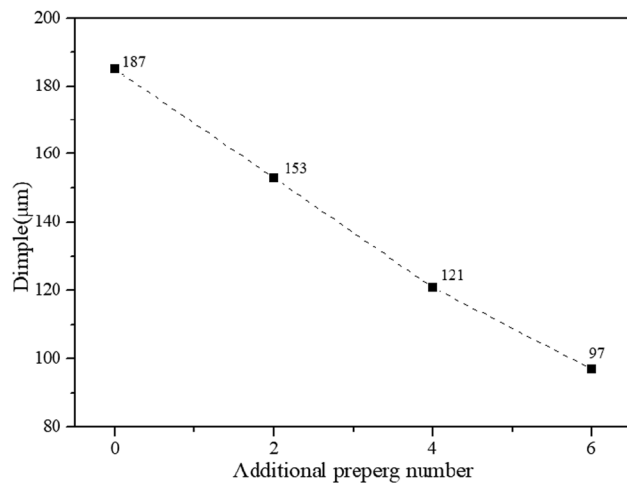


Figure 6: Dimple of BGA area in condition of different additional prepreg quantities.

dimple almost linearly decreases with the increase in the additional prepreg numbers. When additional six prepregs are added, the dimple of BGA area is 97.1 μm, as shown in Figure 7, which is satisfied with the load board quality requirements.

3.2 Coverage and reliability improvement of through hole metallization in BGA area

On the one hand, as an insulating dielectric material used for high-speed signal transmission, M6G or IT968 is difficult to desmear before electroless plating. The poor desmear which is performed by alkaline potassium permanganate

solution results in the lack of seed layer in through hole, as shown in the red solid rectangular mark of Figure 8(a). The plasma treatment with CF_4 and O_2 for 50 min after desmear can obviously improve the seed layer coverage in through hole. It is contributed to the modification of resin end-group [35,36]. The self-developed electroless thick copper plating of 18 μm can further improve the seed layer coverage, but the trouble of poor coverage in small size area is still found as shown in Figure 8(b) and (c) (blue dotted rectangle mark). Besides, as presented in the red dotted ellipse mark of Figure 8(d) and (e), the metallization by electroless thick copper plating in through hole shows poor reliability after more than three times 288°C thermal shock by solder float. The copper layer crack mainly occurred at the position of glass fiber of insulating dielectric layer and junction between electroless copper layer and inner layer copper pad. Furthermore, in Figure 9, the microtopography of electroless thick copper layer in through hole wall reveals that there is a small crack at the position of glass fiber (blue dotted rectangle mark) and inner layer copper pad (red dotted rectangle mark). According to the theory of microscopic fracture mechanics, the initial crack leads to easier crack propagation, which results in deterioration of material life [39–41,46–48].

The through hole metallization which is realized by electroplating copper (13 μm) on electroless thick copper plating (5 μm) can solve the initial crack trouble of electroless thick copper (18 μm). In Figure 10, there is no crack at the position of inner layer copper pad and glass fiber. Electroplating copper shows great coverage capability to the micro crack of electroless thick copper layer. Due to the

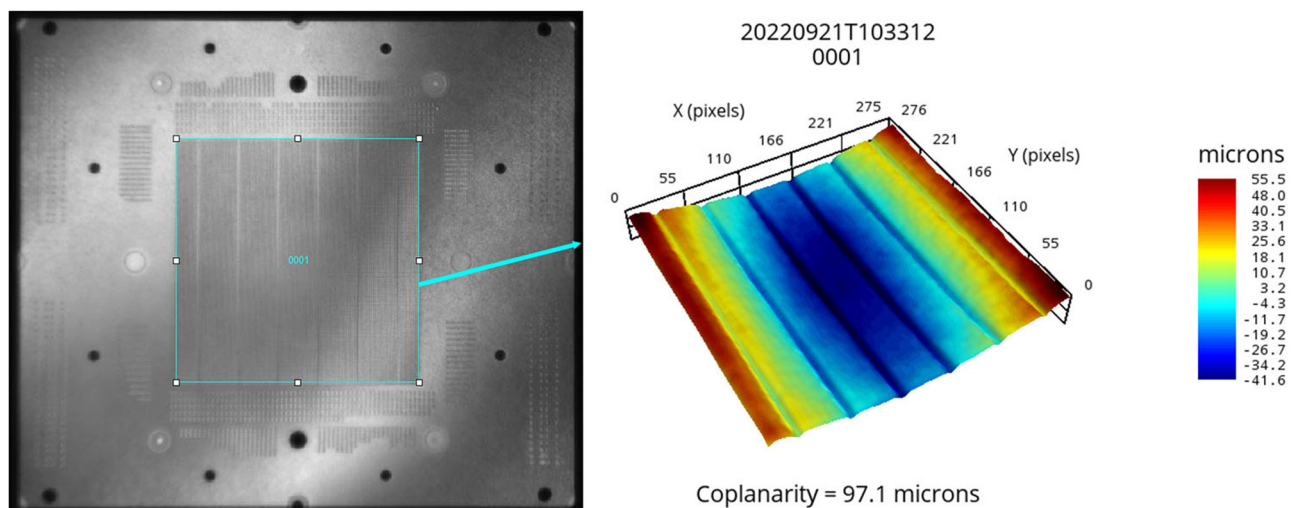


Figure 7: Dimple of BGA area in condition of six additional prepregs.

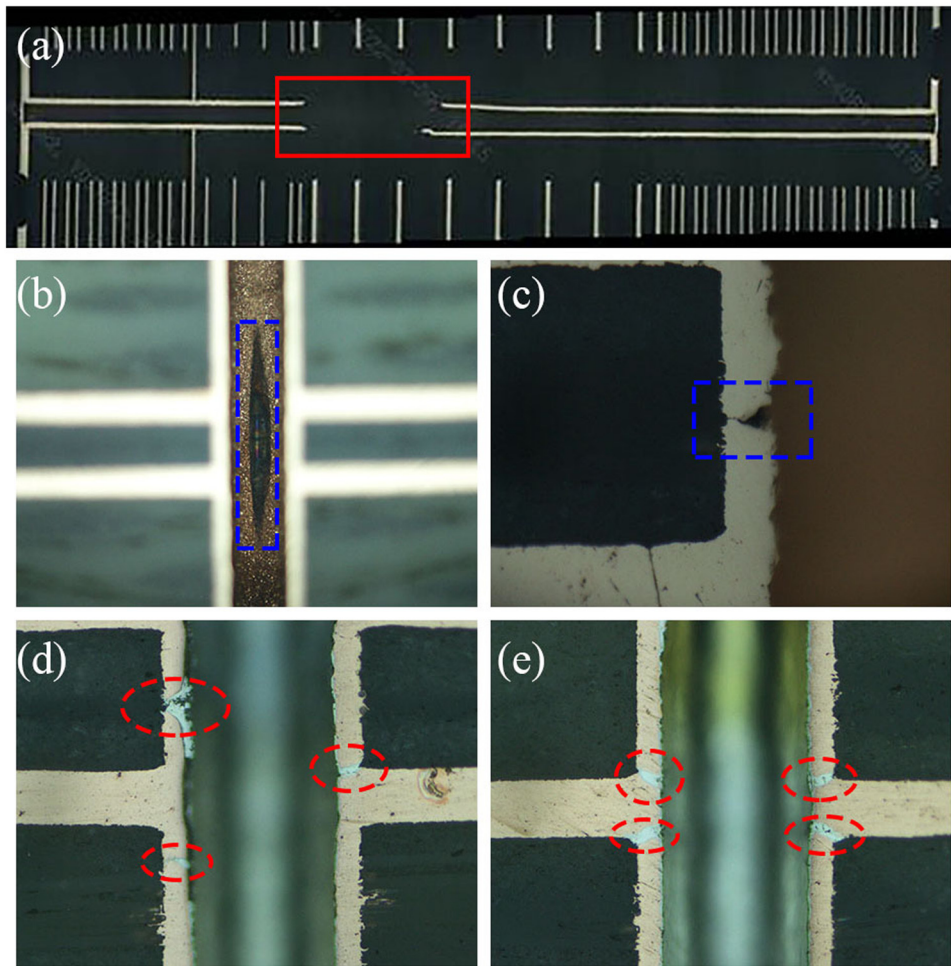


Figure 8: Reliability risk of through hole metallization, (a) poor electroless copper layer coverage in through hole wall, (b and c) poor electroless thick copper layer coverage in through hole wall, (d and e) crack of electroless thick copper layer after 288°C solder float.

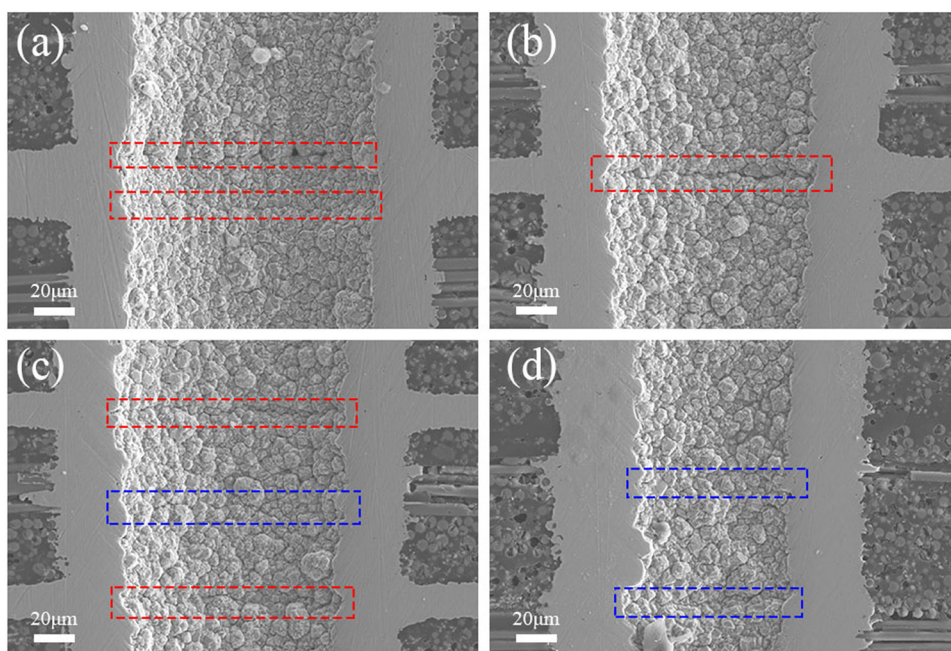


Figure 9: Microcrack of electroless thick copper layer. (a) double microcrack at position of thick inner layer pad, (b) single microcrack at position of thin inner layer pad, (c) microcracks at position of inner layer pad and glass fiber, and (d) microcracks at position of glass fiber.

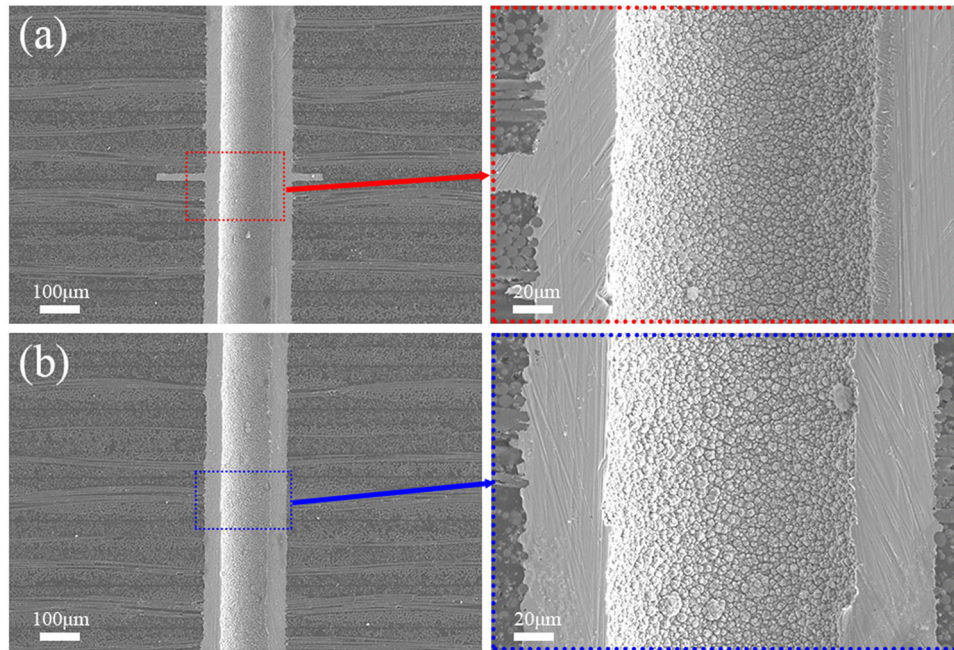


Figure 10: Microstructure of electroplating copper layer (13 μm) on electroless thick copper layer (5 μm) at the position of (a) inner layer pad and (b) glass fiber.

great coverage capability of electroplating copper, there is also no lack of metallization layer in the through hole, as shown in Figure 11(a). The thermal shock reliability of metallization layer including 5 μm electroless thick copper and

13 μm electroplating copper is performed by a load board vehicle with 126 layers and 8.3 mm thickness. Figure 11(b) is the result of metallization layer capability test (based on IT968) after 12 times 288°C solder float. Although there are

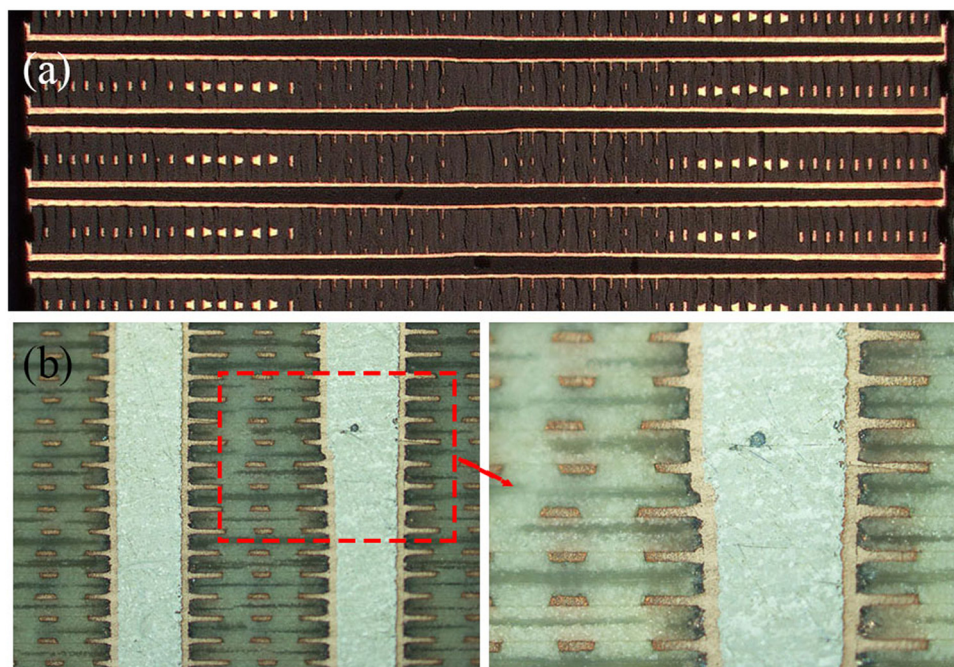


Figure 11: (a) Cross section image and (b) reliability after 288°C solder float of through holes at BGA area after metallization by electroplating copper layer (13 μm) on electroless thick copper layer (5 μm).

more inner layer copper pads, which means greater crack risk, no crack is found in the metallization layer.

On the other hand, the stress and strain of copper layer in the through hole after 288°C solder float is simulated in the condition of different insulating dielectric materials. Figure 12(a) is the simulation result of through hole with 18 μm copper metallization layer. At the same position of copper layer in through hole, although the temperature distribution shows little difference, the Von Mises stress and logarithm strain in condition of IT968 are both smaller than those in the condition of M6G. It indicates that the thermal shock reliability of through hole metallization layer is better when IT968 is used than when M6G is used [48–51]. Figure 12(b) is the result of through hole with 18 μm copper metallization layer after resin filling and outer layer patterning. First, the temperature distribution is different when IT968 or M6G is used, which is

different from the model of through hole with only 18 μm copper metallization layer in Figure 12(a). Compared to M6G, the temperature distribution of copper layer is lower at the same position of through hole in the condition of IT968. It is probably attributed to the specific heat capacity of IT968 being larger than that of M6G. Accordingly, the difference of Von Mises stress and logarithm strain between using IT968 and M6G reveals that the thermal shock reliability of through hole metallization layer after resin filling and outer layer patterning is better when IT968 is used than when M6G is used. Figure 12(a) and (b) both present that IT968 is better than M6G for the thermal shock reliability of through hole metallization layer. Besides, Figure 12 also shows that the Von Mises stress and logarithm strain decrease when through hole is filled with resin. It indicates that hole filling by resin is an effective approach to reduce the reliability risk of copper interconnection structure in load board.

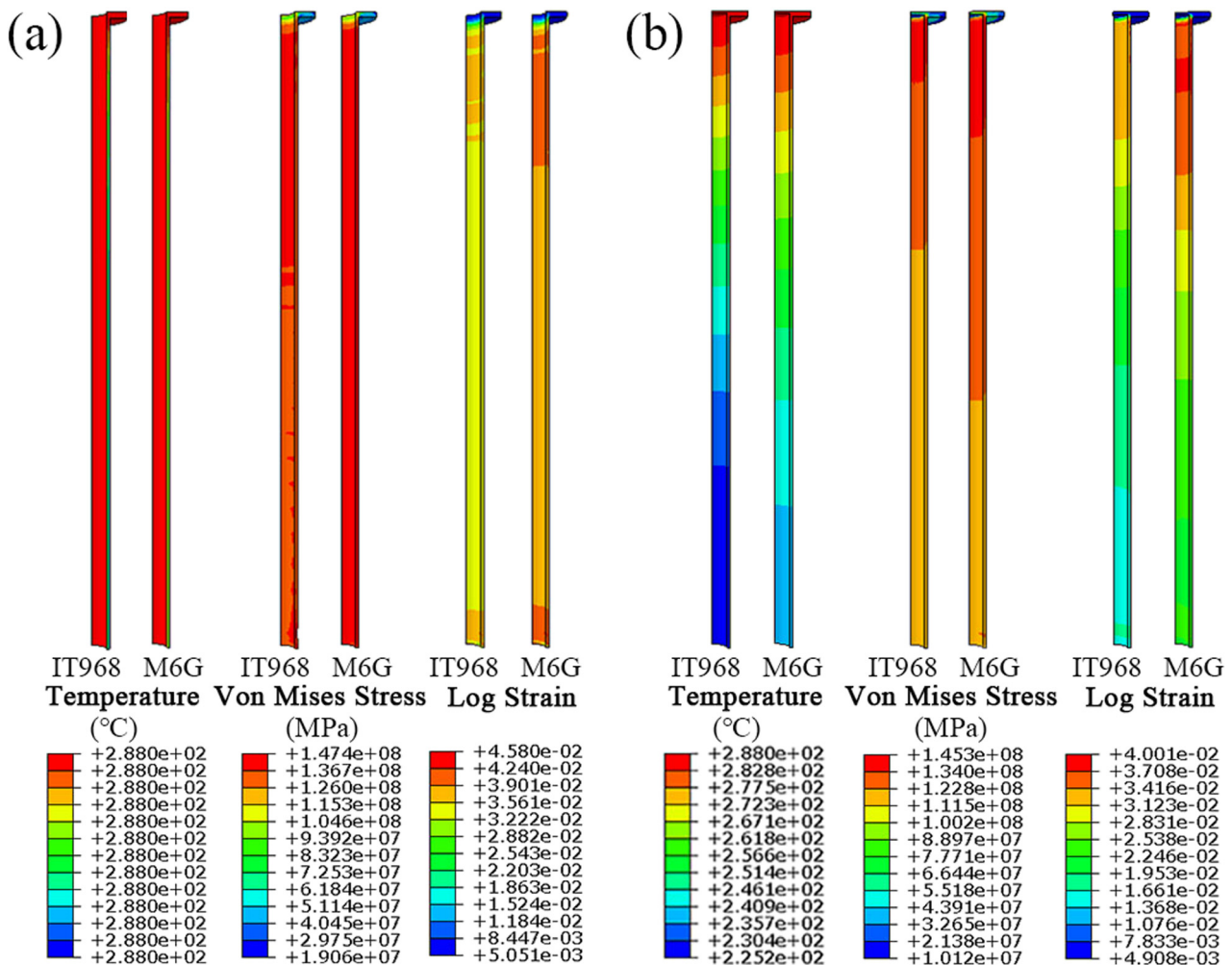


Figure 12: Temperature, stress and strain simulation of (a) metallized through hole before resin filling and (b) metallized through hole after resin filling and outer layer patterning after 288°C solder float.

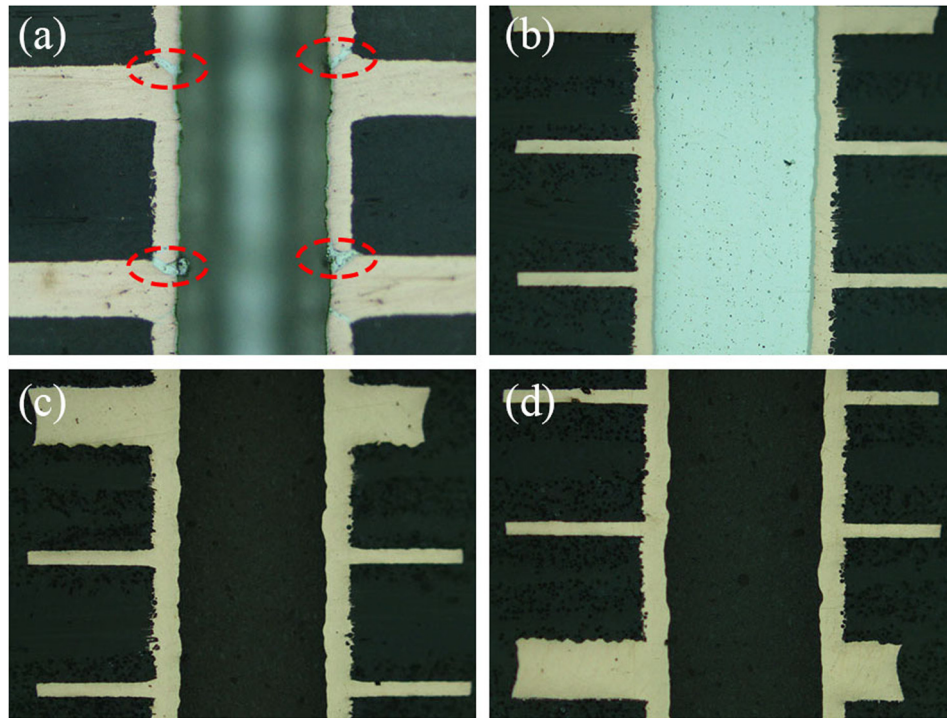


Figure 13: Cross section image of metallization layer in through hole (a) without resin filling based on M6G, (b) without resin filling based on IT968, (c) with resin filling based on M6G, and (d) with resin filling based on IT968 after three times 288°C solder float.

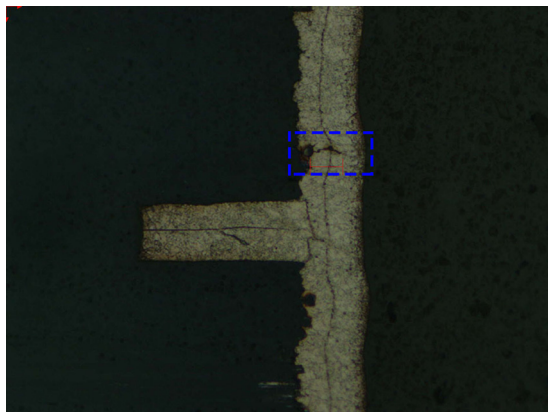


Figure 14: Microcrack through electroless thick copper layer in the condition of through hole with resin filling based on M6G after three times 288°C solder float.

Figure 13 presents the metallized through hole in BGA area after three times 288°C solder float, which agrees with the simulation results in Figure 12. The diameter and pitch of through hole in load board vehicle with 62 layers and 7 mm thickness is 0.2 and 0.6 mm, respectively. The metallization layer in through hole is prepared with 18 μm (5 μm electroless thick copper and 13 μm electroplating copper). When load board is prepared based on M6G, serious through cracks are found in the through hole without resin

filling, as shown in Figure 13(a), but no through crack is found in the through hole without resin filling, as shown in Figure 13(c). When load board is prepared based on IT968, as shown in Figure 13(b) and (d), no crack is found in the condition of both with and without resin filling. The Von Mises stress and strain simulation results in Figure 12 also predict these trends. In Figure 12, the through hole with resin filling based on M6G shows greater crack risk compared to that based on IT968. In the load board vehicle based on M6G, although no through crack is found, there is a certain probability of microcrack through electroless thick copper layer, as shown in Figure 14, especially in the position of eighth of thickness from board surface.

Based on the results of large size BGA area dimple reducing and through hole metallization layer coverage and thermal shock reliability improvement, Figure 15(a) presents the cross section of BGA area with 0.2 mm diameter and 0.6 mm pitch through hole in a load board with 62 layers and 7.53 mm thickness. Figure 15(b)–(d) are the cross section of through hole with 18 μm copper metallization layer (13 μm electroplating copper layer on 5 μm electroless thick copper seed layer), resin filling, and outer layer patterning after 3 times, 8 times, and 12 times thermal shock test, respectively. The load board vehicle with 126 layers and 8.3 mm thickness is prepared based on IT968. The through hole diameter in this load board

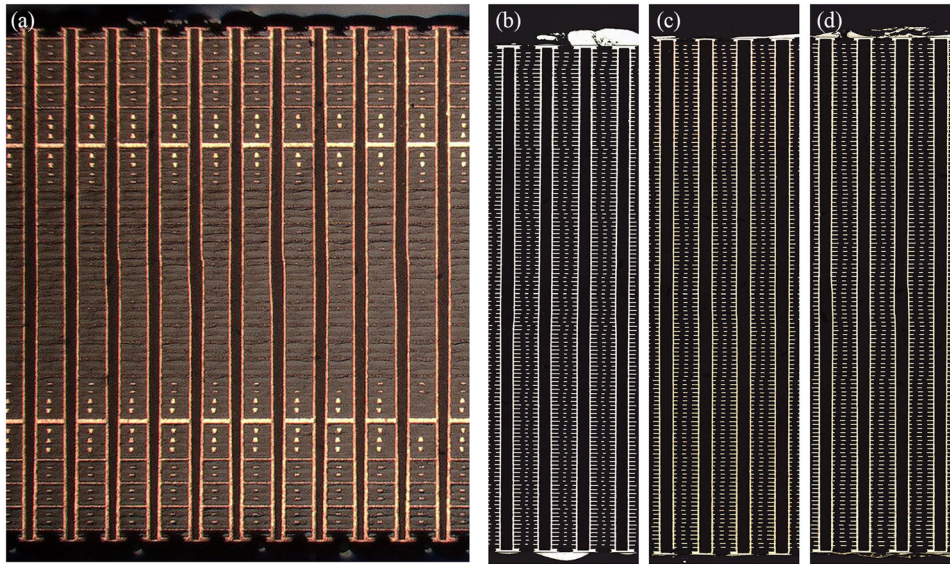


Figure 15: (a) Cross section of through holes at BGA area on load board based on IT968 and reliability test after (b) 3 times (c) 8 times, and (d) 12 times 288°C solder float.

vehicle is 0.25 mm. Figure 13 shows the good assemblability and interconnect structure reliability of the load board used for high performance IC test.

4 Conclusion

In this work, the dimple of 70 mm × 70 mm BGA area after hot lamination and reliability of through hole metallization in BGA area are investigated for load board manufacture. Due to low residual copper ratio in BGA area, coupled with too thick copper pattern, the prepreg is not enough to fill the BGA area completely. Additional prepreps at BGA area are employed to reduce the dimple after hot lamination. The cross section and surface microtopography of copper metallization layer in through hole is investigated for improving the coverage and reliability of interconnection structure. Two insulating dielectric materials, including IT968 and M6G, are compared by simulation for stress and strain of through hole copper metallization layer after 288°C solder float. The following conclusions can be obtained from this work:

- 1) The dimple of BGA area decreases from 184.3 to 97.1 μm when six additional prepreps with 60 mm × 60 mm size are used.
- 2) Plasma treatment before electroless copper plating and self-developed electroless thick copper plating improves the coverage of copper metallization on through hole wall.
- 3) The microcracks of electroless copper layer at the position of glass fiber of insulating dielectric layer and

junction between electroless copper layer and inner layer copper pad, which leads to serious crack after 288°C solder float, are well covered by subsequent electroplating copper layer.

- 4) The simulation results of metallized through hole before and after resin filling both point out that IT968 is better than M6G for the thermal shock reliability of through hole metallization layer.
- 5) The simulation results also reveal that the resin filling is an effective approach to reduce the reliability risk of copper interconnection structure in load board.
- 6) A load board vehicle with 126 layers and 8.3 mm thickness based on IT968 shows good interconnection structure reliability after 12 times 288°C solder float.

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