

Yao-Feng Chang¹ / Burt Fowler² / Ying-Chen Chen¹ / Fei Zhou¹ / Xiaohan Wu¹ / Yen-Ting Chen¹ /
Yanzhen Wang¹ / Fei Xue¹ / Jack C. Lee¹

Resistive switching characteristics and mechanisms in silicon oxide memory devices

¹ Department of Electrical and Computer Engineering, The University of Texas at Austin, Austin, TX 78758, USA, E-mail: yfchang@utexas.edu

² PrivaTran, LLC, Austin, TX 78746 USA

Abstract:

Intrinsic unipolar SiO_x-based resistance random access memories (ReRAM) characterization, switching mechanisms, and applications have been investigated. Device structures, material compositions, and electrical characteristics are identified that enable ReRAM cells with high ON/OFF ratio, low static power consumption, low switching power, and high readout-margin using complementary metal-oxide semiconductor transistor (CMOS)-compatible SiO_x-based materials. These ideas are combined with the use of horizontal and vertical device structure designs, composition optimization, electrical control, and external factors to help understand resistive switching (RS) mechanisms. Measured temperature effects, pulse response, and carrier transport behaviors lead to compact models of RS mechanisms and energy band diagrams in order to aid the development of computer-aided design for ultralarge-v scale integration. This chapter presents a comprehensive investigation of SiO_x-based RS characteristics and mechanisms for the post-CMOS device era.

Keywords: Resistive switching mechanism, silicon oxide, proton exchange reaction

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1 Introduction

Floating gate (FG) memory has been the primary structure used for nonvolatile memory (NVM) devices since its invention in 1967 by D. Kahng and S. M. Sze and has been widely employed in the portable electronic products such as mobile phones, digital cameras, notebook computers, mp3 players, and USB flash drives. The operating principle of conventional NVM is based on the use of polycrystalline silicon as an FG to store charges injected from a channel [1]. However, as device size continues to shrink, the typical flash memory device will continue to suffer from degraded retention and endurance [2]. In order to solve these problems, researchers have presented two main methods to improve memory devices with different storage technologies. The first is to change the storage layer without changing the device structure, and the second is to propose novel structures. In order to change the storage layer, either silicon nitride [3] or discrete nanocrystals [4, 5] have been employed as storage cells. However, making changes to the storage layer cannot fully resolve issues related to scaling down device size and increasing program/erase speed. Therefore, researchers have considered new storage layers and novel structures in NVM devices to replace the conventional FG device. New NVM devices must exhibit faster program/erase speeds and higher endurance. As for device size scale-down requirements [6–11], new devices should be compatible with a cross-point structure. Over the past decade, numerous potential memory structures have been proposed, with some being transferred into production lines, such as phase change memory (PCM), magnetic random access memory (MRAM), and ferroelectric random access memory (FeRAM). More recently, resistance random access memories (ReRAMs) have gained significant research interest as an alternative for next-generation NVM due to their high density, low cost, low power consumption, fast switching speed, and simple cell structure [12–22]. In addition, ReRAM technology can achieve program/erase speeds as high as static random access memory (SRAM) and densities as large as dynamic random access memory (DRAM), while retaining the non-volatile properties of flash memory; therefore, ReRAMs demonstrate very good potential for replacing NAND flash, a type of FG memory, to become the next-generation NVM.

The structure of ReRAM devices consists of sandwiched metal/insulator/metal (MIM) layers. By applying voltage or current, the resistance of the device can be changed, thereby providing data storage capability. ReRAM first originated from Hickmott in the 1960s; he discovered that the resistance of AlO_x could be modified after applying a voltage or current. The logic state “0” or “1” is defined by different resistance values and

Yao-Feng Chang is the corresponding author.

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can be read by applying a low voltage to measure the resistance state. In recent years, resistive switching characteristics of a large variety of materials have been reported, including binary metal oxides such as NiO, CuO, and HfO_x . ReRAM devices exhibit good nonvolatile characteristics, and the stored data are retained until the next data are written. Characteristics such as low operating voltage, fast program/erase speed, and good scale-down capability make ReRAM a suitable candidate for the next-generation NVM. Hence, ReRAM is gaining significant interest in academia and industry for its high practicality and potential for commercial use.

In this chapter, SiO_x -based ReRAM characteristics, mechanisms, and potential applications are reviewed [23–49]. Deep insights into resistive switching characteristics are provided. Possible resistive switching mechanisms are investigated, including an example of RS model based on proton exchange reactions that describe device transitions between high-resistance state (HRS) and low-resistance state (LRS). These studies regarding novel SiO_x -based ReRAM and related physical mechanisms represent a significant contribution to the development of next-generation NVM.

2 Results and discussion

2.1 Device structure, materials, and electrical control for SiO_x -based ReRAM

2.1.1 Post-deposition anneal and polarity effects

Recent reports by Yao et al. on SiO_x -based resistive switching in vacuum indicate that this traditionally passive material can be converted to an active memory material by external electrical activation [35, 36]. Although many resistive switching mechanisms have been reported for various materials [37, 38], the exact switching mechanisms in SiO_x -based materials have yet to be identified and may be different than traditional materials. Therefore, characterizing the polarity dependence of device switching is a top priority for the unipolar, SiO_x -based resistive switching memory. Specifically, analyzing and understanding device RESET switching parameters will help develop a resistive switching model. In Figure 1, SiO_x -based resistive switching memory is realized by fabricating a tantalum nitride (TaN)/ SiO_2 /heavily doped n-type (n^{++}) Si-substrate structure. Device switching characteristics and stability were investigated with and without a postdeposition anneal (PDA). The polarity dependence of switching characteristics suggests that the switching region is located at the cathode side, potentially due to the asymmetrical thermal-dissipation structure of the TaN/ SiO_2 / n^{++} Si device. Also, data retention tests in the HRS and LRS for over 10^4 seconds confirm the nonvolatile nature of the device. Testing several different device structures enables the development of a possible resistive switching model to aid characterizing SiO_x -based devices for use in future ReRAM applications.

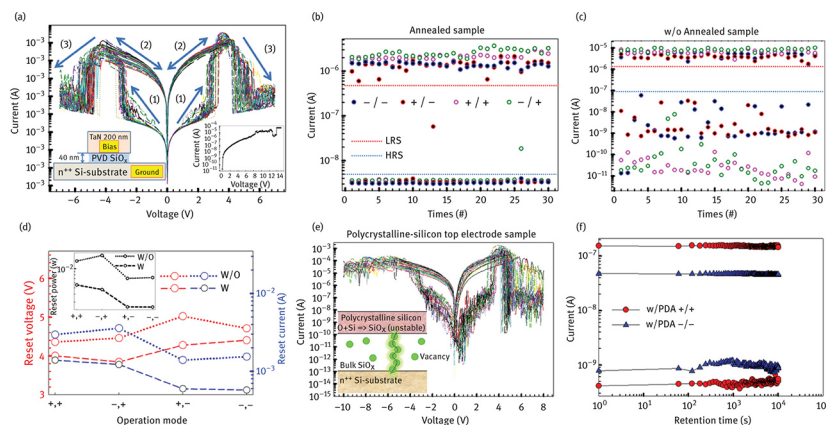


Figure 1: Thirty cycles of resistive switching behavior in samples with PDA. Arrows indicate voltage sweep directions. Left and right insets show a schematic representation of the TaN/ SiO_2 / n^{++} Si-substrate structure and an I - V plot of electroforming data, respectively. (b) and (c) Polarity dependence of LRS and HRS distributions across 30 cycles for samples (b) with and (c) without 5 min 500°C PDA in O_2 . In (b), $-/-$ means negative SET/negative RESET. (d) Polarity dependence of RESET voltage, RESET current, and RESET power (inset) for samples with and without PDA. (e) Polycrystalline-silicon top electrode device switching characteristics and O^- ion reaction with Si in polycrystalline-silicon electrode to form SiO_x (inset). (f) Retention test at room temperature for samples without PDA in positive and negative polarity conditions.

2.1.2 Horizontal and vertical device structure designs, composition optimization (SiO_x , $x < 2$), and electrical control characterizations

In Figure 2, the oxygen content effect in SiO_x -based ReRAM has been investigated by controlling the O_2 flow rate during reactive sputtering of Si in an O_2 ambient. It has been found that device yield, switching characteristics, and stability are all improved for device layers with near-stoichiometric oxygen content (i.e., $x \sim 2$). The effects of SiO_x thickness, device area, and multilevel operation by controlling set compliance current and reset voltage suggest that the switching region is located at the interface and is localized rather than occurring uniformly throughout the bulk SiO_x layer. Also, the current transport behaviors in the HRS and LRS have been studied. A general current flow model for unipolar SiO_x -based resistive switching memory has been proposed, which provides a simple physical concept to describe RS behavior and provides additional insights into optimization of ReRAM devices.

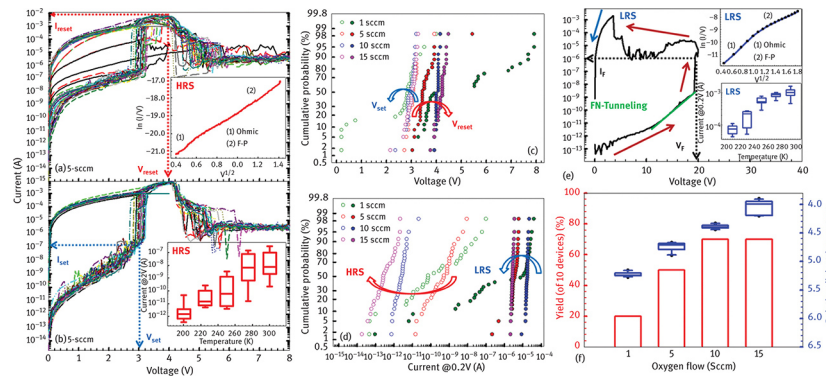


Figure 2: Thirty cycles of unipolar switching behaviors of samples deposited using reactive sputtering with (a) 5 sccm of O_2 and (b) 10 sccm of O_2 with compliance current of 1 mA applied during the set process. Top and bottom insets show a plot of $\ln(I/V)$ versus $V^{1/2}$ and a plot of current versus temperature in HRS. Distribution of (c) $V_{\text{SET}}/V_{\text{RESET}}$ and (d) HRS/LRS current as a function of O_2 flow. (e) Electroforming I - V response of 15-sccm (Standard cubic centimeter per minute) sample. Right top and right bottom insets show a plot of $\ln(I/V)$ versus $V^{1/2}$ and a plot of current versus temperature in LRS. Arrows indicate voltage sweep directions. (f) Device yield and relative dielectric constant as function of oxygen flow rate in SiO_x deposition process.

2.1.3 Ambient effects and bimodal failure phenomenon

In addition to excellent insulating properties, SiO_x -based materials have recently demonstrated resistive switching phenomena in both vacuum and atmosphere ambients. The devices exhibit unique unipolar operating characteristics where turn-off voltage is the same as or larger in magnitude than the turn-on voltage. In addition, resistive switching occurs only in nonoxidizing ambients. Although several potential resistive switching mechanisms have been reported for SiO_x -based devices, the exact switching mechanisms are still not well understood. In Figure 3, the sensitivity to oxygen in SiO_x -based ReRAM has been investigated by controlling the ambient gas pressure and monitoring resistive switching characteristics. Operating stability measurements in vacuum, nitrogen, and oxygen-nitrogen ambients show that SiO_x -based ReRAM is sensitive to oxygen partial pressure, where resistive switching is temporarily disabled for O_2 partial pressures above 2 Torr. Interestingly, a subsequent vacuum recovery process restores normal functionality. The statistical distribution of electrical parameters in the oxygen-induced failures can be described using bimodal Monte Carlo simulations and additional failure analysis. Potential solutions for a unique resistive-switching-type oxygen sensor and packaging methods for SiO_x -based ReRAM are described for the development of clear design criteria for future applications.

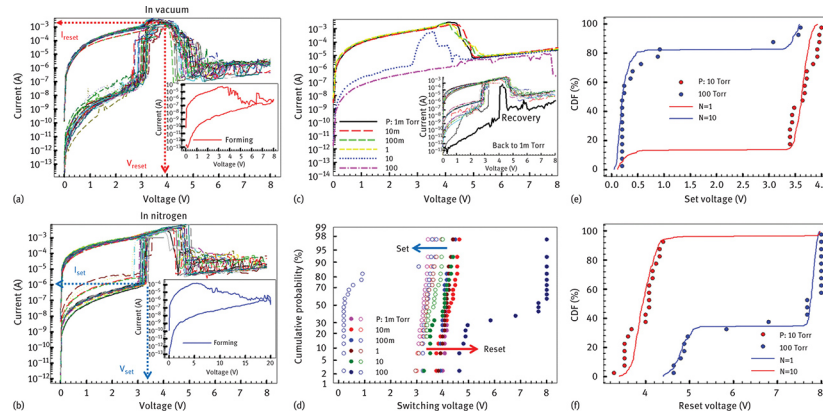


Figure 3: The resistive switching behaviors and forming processes (insets) in (a) vacuum and (b) N_2 ambients. (c) Average current for 20 SET/RESET cycles for different pressures of 20% O_2 - N_2 and the device recovery process in vacuum (inset). (d) Cumulative probability of switching voltage as function of 20% O_2 - N_2 pressure. Initiation of resistive switching failures above 10 Torr of 20% O_2 - N_2 mixture showing the cumulative distribution function using bi-modal Monte Carlo simulation fitting for (e) SET and (f) RESET voltage.

2.1.4 Edge and bulk device structures, an unusual backward-scan effect, and circuit-level simulation

Several “extrinsic” SiO_x -based resistive switching behaviors have been reported, which may result from doping-induced filament formation during the fabrication process or highly diffusive, stacked electrode structures, but the “intrinsic” switching mechanisms are still not well understood. ReRAM devices using SiO_x as the active switching medium have unusual electrical characteristics where resistive switching occurs only in nonoxidizing ambients and a unique unipolar operation where RESET voltage is typically larger in magnitude than SET voltage [33]. Current increases with temperature and is fairly independent of device area and SiO_x thickness, indicating that switching occurs in a localized region along a conductive filament. Device structures typically incorporate an etched sidewall to increase electroforming yield. In previous reports, the unique unipolar operation of SiO_x -based ReRAM has been investigated by controlling the external resistance using a series transistor (1T) and monitoring resistive switching characteristics. A nonedge SiO_x device demonstrates that resistive switching can occur in bulk SiO_x materials and provides additional fabrication flexibility. Thermal anneal of bulk devices in reducing ambient improves device performance by hydrogen incorporation. An unusual backward-scan effect, where the device state is determined by the duration of the reverse sweep, is examined by DC and AC pulse measurements to quantify the requirements for programming duration during the RESET process (Figure 4). The switching behavior of the backward-scan effect is incorporated into Verilog-A simulations to characterize integration strategies for future circuit-level applications.

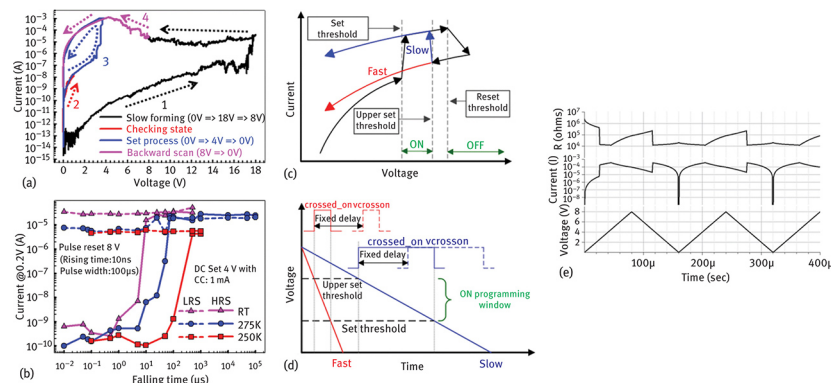


Figure 4: The backward-scan effect during a DC sweep: (1) Forming voltage sweep with slow rate (1,000 points in sweep range); (2) check of device state using a DC sweep from 0 V to 1 V; (3) SET process using a 4 V forward/reverse DC sweep with 1 mA compliance current limit; and (4) backward-scan effect in the SiO_x device. (b) The backward-scan effect using AC pulses with controlled falling times versus temperature. The fast (red) and slow (blue) backward voltage sweeps are plotted in (c) I - V and (d) V - t form. In (d), the crossed_on and vcrosson signals linked to the time axis are used to determine whether the device will switch from the OFF to ON state. (e) Resistance (R), current (I), and voltage (V) simulation results demonstrating that the device switches from OFF to ON state during a slow backward voltage sweep.

2.1.5 Integrated one diode–one resistor (1D–1R) nanopillar architecture

By considering the static power consumption and sneak-path issues in large-scale crossbar array designs, a Schottky diode is not suitable for portable electronics due to its high reverse-bias leakage current and relatively low reverse-bias breakdown voltage as compared to a Si-based PN-diode or transistor. For example, the reverse leakage current of Schottky diodes can increase dramatically with temperature to the point of a thermal-runaway situation, potentially resulting in instability issues and readout failures. In Figure 5, a Si diode (1D) with low reverse-bias current is integrated with a SiO_x -based memory element (1R) using nanosphere lithography (NSL) and deep-Si-etching (DSE) to pattern a $\text{P}^{++}/\text{N}^+/\text{N}^{++}$ epitaxial Si wafer. The self-aligned process forms a high-density, large-scale nanopillar (NP) array architecture. Compared with conventional photolithography or direct-writing methods (e.g., electron beam lithography or focused ion beam milling), NSL is demonstrated as a low-cost (maskless), high-throughput alternative technique to pattern large areas. The nanostructures fabricated using NSL can be well controlled in shape, size, and interpillar spacing through direct assembly of polymer nano-spheres on the wafer scale. Performance of 1R and 1D–1R structures is characterized and shows that the integrated nanopillar 1D–1R configuration offers low static power for suppression of sneak-path issues. The work reported here provides an efficient fabrication process and low reverse-bias current in a SiO_x -based 1D–1R configuration for potential use in future ultra-large-scale NVM applications.

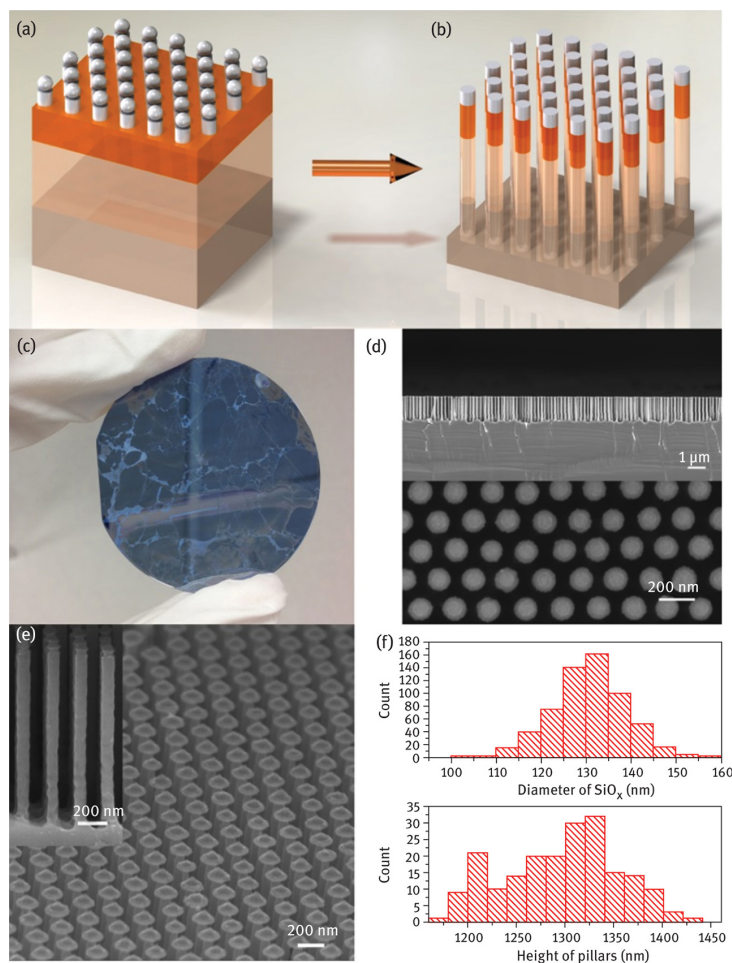


Figure 5: 1D–1R fabrication process using DSE and device electrical characteristics: (a) Transfer of NSL pattern to SiO_x hard-mask deposited on epitaxial $\text{P}^{++}/\text{N}^+/\text{N}^{++}$ Si wafer. (b) DSE process in Bosch mode to form a self-aligned 1D–1R NP architecture. (c) Wafer scale and (d) and (e) SEM images of 1D–1R NPs. (f) Statistical distribution of nanopillar diameter and height.

2.2 Modeling of SiO_x -based resistive switching mechanisms

2.2.1 Oxide stoichiometry effects on reversible switching and program window optimization

The achievements for intrinsic unipolar SiO_x -based ReRAM include (1) high device yield, forming-free operation, reduced operating voltage, and excellent stability; (2) pulsed programming in the 50-ns regime for integrated

1D–1R cross-point arrays and sub- μA operating current in high-density 1D–1R architectures. However, characterization and modeling of current transport behaviors, defect transformations, energy band diagrams, and self-compliant mechanisms are not well understood. We analyze the effects of device structure, electrode material, SiO_x thickness, and device area on electrical characteristics and confirm that RS occurs in a localized region along a conductive filament (CF), as shown in Figure 6. A physical model consistent with the observed RS I – V response is proposed. Several studies have used transmission electron microscopy to document the presence of Si nanocrystals within the CF, but it is not yet clear whether RS is the result of an overall increase in nanocrystal size or whether switching occurs in “GAP” regions in between nanocrystals. Most models of ReRAM switching involve the drift or diffusion of O^{2-} ions (or oxygen vacancy defects), but these models cannot explain the unipolar I – V response or the ambient effects on RS observed in the SiO_x device. Our RS model differs from most conventional models by considering that the defects responsible for RS may remain localized within the switching region so that RS occurs when a collection of defects are driven between conductive and nonconductive forms. Based on the reported electrical and structural properties of known SiO_x defects, we further describe how proton exchange reactions can dramatically alter the conductivity of specific defects, leading to a model where the LRS has a large concentration of conductive defects within the switching region, and, conversely, when the device is programmed to the HRS, most of the defects are converted to their nonconductive form. The electrically conductive hydrogen bridge (Si–H–Si) is viewed as the most likely defect responsible for the LRS. Electrochemical reactions that form the nonconductive $(\text{SiH})_2$ defect are discussed as potential mechanisms that enable localized switching without incorporating ion diffusion or drift mechanisms into the model. Our experimental results and RS model provide insights into device electrical characteristics and charge transport and may help identify localized, defect-driven switching mechanisms in SiO_x -based ReRAM devices. Although the models described herein provide reasonable, accurate descriptions of RS in SiO_x materials, it must be noted that direct evidence for the defects used in the models is likely to be very difficult, if not impossible, to obtain. Until direct evidence is found, the models represent a reasonable working hypothesis regarding RS mechanisms in SiO_x materials.

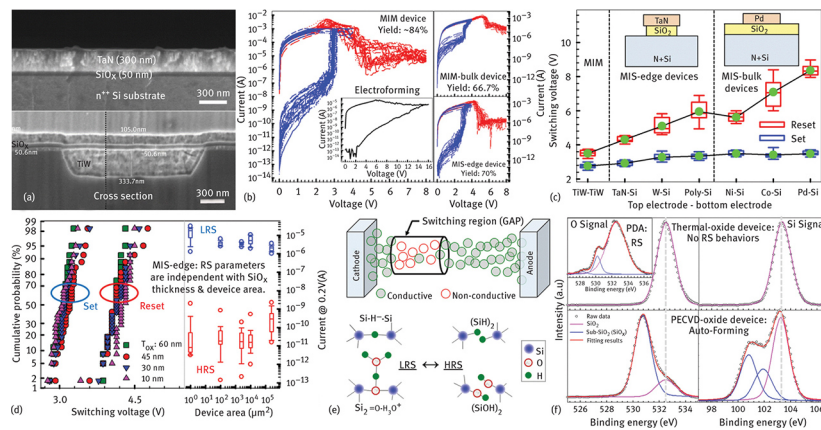


Figure 6: SEM images of TaN/ SiO_x / $n^{++}\text{Si}$ (MIS) structure in upper panel and TiW/ SiO_x /TiW (MIM) structure in lower panel. The MIM image is a composite (dashed line) showing the two ends of a single, 20- μm -wide, planarized TiW electrode. (b) Thirty cycles of unipolar switching I – V plots for MIM (electroforming process shown in the inset), MIS-bulk, and MIS-edge devices with corresponding yield labeled. (c) Effects of electrode material on SET and RESET switching voltages in MIM, MIS-edge, and MIS-bulk devices. The inset shows schematic of device structures of Mis-bulk and Mis-edge devices mean and represent in Fig.6 (c). (d) RS parameter dependence on SiO_x thickness and device area in MIS-edge devices. (e) Physical representation of conductive filament with switching region (GAP) containing a mixture of conducting and nonconducting defect complexes. (b) Hypothesized defect complex in LRS (left) and HRS (right) representing potential electrochemical reaction products involved in switching, where the transfer of a single proton between two defects is responsible for RS. (f) $\text{O}-1_s$ and $\text{Si}-2_p$ X_{PS} spectra and fitting results for low-pressure chemical vapor deposition thermal oxide, sputtered oxide with postdeposition anneal (PDA) treatment, and plasma-enhanced chemical vapor deposition oxide.

2.2.2 Thermal effects on charge transport and potential for multilevel programming

ReRAM devices can potentially be scaled to smaller sizes than NAND flash memory and are compatible with three-dimensional (3D) architectures, making ReRAM very attractive for future high-density production. Another way to improve storage density is through multilevel data storage where the memory element is capable of storing more than a single bit of information. For example, a cell that stores four states will yield two bits of information per cell. Therefore, a multilevel cell provides higher bit/ cm^2 density with lower cost and more

economical manufacturing. Multistate storage is achieved in ReRAM by controlling the electrical programming conditions and requires that multiple resistance states have low programming variance so that each state is distinguishable from the others. Many RS mechanisms related to multilevel operation have been reported for various material systems and have successfully been incorporated into device operating models. One multilevel programming method that has been explored is using a compliance current limit (CCL) during the SET process [46], where an increase in CCL induces a more-robust, lower-resistance conductive filament and smaller CCL values are used to program a range of higher resistances. A second programming method is used to achieve higher resistance values by controlling the RESET voltage magnitude [46], where LRS/HRS current ratios as high as 10^8 can potentially be achieved.

To understand the RS mechanism, temperature dependence of device current provides additional information related to charge transport characteristics, such as electron energy barriers, average hopping distance, and the relative permittivity of the switching medium. We propose that the distinctive unipolar properties may result from proton exchange reactions during switching events that cause defect transformations between conductive and nonconductive forms (see Figure 6e). Here, specific defect energy levels are correlated to the switching transitions in the $I-V$ response and the current overshoot phenomenon observed in the LRS [46], leading to energy band diagrams that further illustrate the switching transitions (Figure 7). The presented experimental results and physical switching model provide possible explanations for the distinctive unipolar operating characteristics of intrinsic SiO_x -based resistive switching memory.

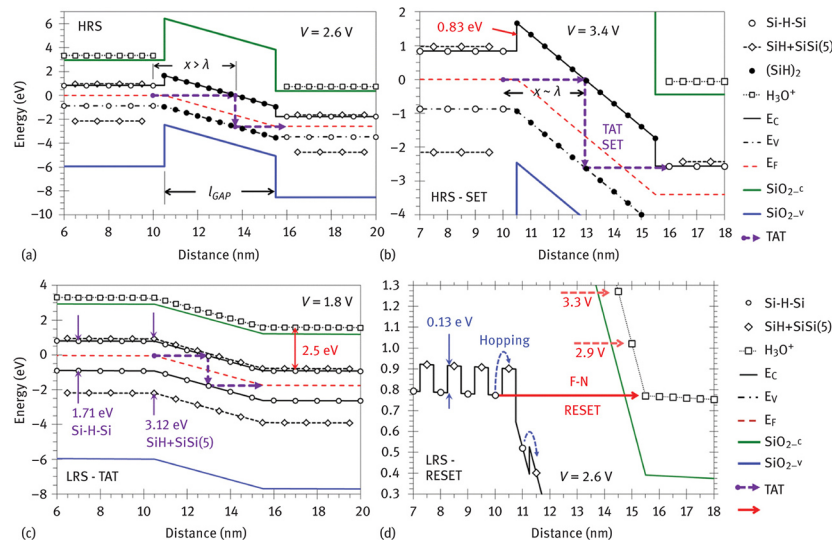


Figure 7: Energy band diagrams plotting electron potential energy versus distance along the conductive filament in the HRS. (a) Switching region with length $l_{\text{GAP}} = 6$ nm filled with $(\text{SiH})_2$ defects for device biased to 2.6 V. (b) Energy barrier of 0.83 eV to electron transport from Si-H-Si defects into $(\text{SiH})_2$ defects and trap-assisted tunneling (TAT) to induce the SET transition at 3.4 V. Tunneling distance x and characteristic tunneling length λ are labeled in both plots to demonstrate the dependence of x on device bias. (c) Energy band diagram plotting electron potential energy versus distance along the conductive filament in the LRS. Switching region is filled with Si-H-Si, SiH + SiSi(5), and H_3O^+ defects showing available TAT pathway at 1.8 V bias. The effective bandgaps of the Si-H-Si and SiH + SiSi(5) defects and the 2.5 eV separation between Si-H-Si and H_3O^+ are labeled. (d) Energy barrier of 0.13 eV to electron hopping from Si-H-Si to SiH + SiSi(5), and F-N tunneling into H_3O^+ defects to induce the RESET transition at 2.6 V. Increasing bias above 2.6 V allows electron injection into neighboring H_3O^+ defects at 2.9 V and 3.3 V (dashed horizontal arrows), thus forming a conductance gap in the HRS.

3 Conclusion

In summary, we have elucidated device characteristics and defect-related resistive switching mechanisms in intrinsic unipolar SiO_x -based ReRAM. This research investigates SiO_x materials explicitly for use in next-generation nonvolatile memory applications and aims to advance memory device performance through novel device structures and better fabrication techniques.

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