

Research Article

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Impact of severe cracked germanium (111) substrate on aluminum indium gallium phosphate light-emitting-diode's electro-optical performance

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Abstract: Cracked die is a serious failure mode in the Light Emitting Diode (LED) industry – affecting LED quality and long-term reliability performance. In this paper an investigation has been carried out to find the correlation between severe cracked germanium (Ge) substrate of an aluminum indium gallium phosphate (AlInGaP) LED and its electro-optical performance after the Temperature Cycle (TC) test. The LED dice were indented at several bond forces using a die bonder. The indented dice were analysed using a Scanning Electron Microscope (SEM). The result showed that severe cracks were observed at 180 gF onward. As the force of indentation increases, crack formation also becomes more severe thus resulting in the chipping of the substrate. The cracked dies were packaged and the TC test was performed. The results did not show any electro-optical failure or degradation, even after a 1000 cycle TC test. Several mechanically cross-sectioned cracked die LEDs, were analysed using SEM and found that no crack reached the active layer. This shows that severely cracked Ge substrate are able to withstand a $-40^{\circ}\text{C}/+100^{\circ}\text{C}$ TC test up to 1000 cycles and LED optical performance is not affected. A small leakage current was observed in all of the cracked die LEDs in comparison to the reference unit. However, this value is smaller than the product specification and is of no concern.

Keywords: Light-Emitting-Diode; severe cracks; germanium substrate; Electro-optical performance; bond force

1 Introduction

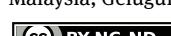
The performance of the Light Emitting Diode (LED) is seriously affected by cracked dies [1]. It is a major concern for the illumination industry [2]. Cracked dies cause reliability issues and to a certain extent, to LED failures [3]. Periodical on-off switching and environmental temperature variation during LED operation will induce cyclic stress on the LED. This cyclic stress will start to cause cracks thus leading to fatigue failure [4]. If the die contains a crack or is pre-damaged during the LED manufacturing processes it will easily fail when it undergoes this stress and strain. The semiconductor process creates such issues. Chen *et al.* [5] observed large deep scratches created by the wafer thinning process which significantly affected the strength of the silicon (Si) die. Cracks at the bottom of die (substrate) can be caused by the Die Attach (DA) process during the die pick up from the mylar tape [6], as illustrated in figure 1a and 1b.

During the die pick up from the mylar tape the ejector pin pushes the die up while the bond head holds the die [7]. When the tip of the ejector pin hits the Ge substrate, plastic deformation will form at the imprint area as illustrated in figure 2. If the bond force exceeds the strength of the die substrate, it will crack. Cracks at the bottom of the die are difficult to detect as it is attached to leadframe with silver phase epoxy glue. It was reported that during the LED operation thermo-mechanical stress in the LED will further aggravate the crack, resulting in total failure of the LED [8–10]. In a related area of research, Guoguang *et al.* [11] reported in his paper that LEDs which failed during operation were found to have large cracks at the active region.

In view of this issue an investigation was carried out to find the correlation between cracks at the bottom of the die

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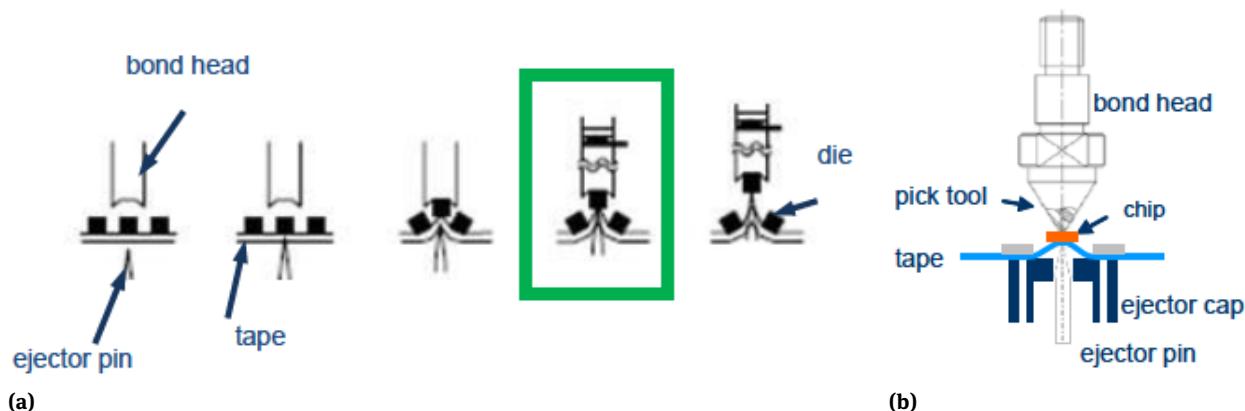


Figure 1: Shows the DA process sequence and details of bond head, chip and ejector pin, (a) illustrate the DA process where the ejector pin pushes and indents the die [6], (b) shows a detailed view of the bond head, chip and ejector pin as illustrated in green box in figure 1a.

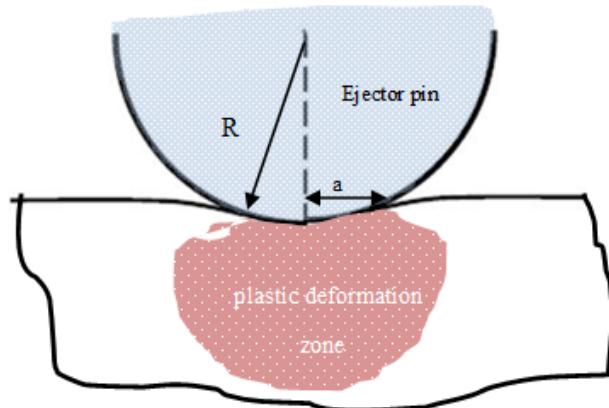


Figure 2: Ejector pin contact to surface of substrate.

substrate to its electro-optical properties and also to study the crack formation against the bond force. In this investigation we have reported on the crack formation on Ge substrates that were bonded at die bond forces from 60 gF to 140 gF. The cracks range from minor to major cracks where the crack lines are very visible under SEM analysis [12]. These die cracked units were subjected to a Power Temperature Cycle Test (PTC) up to 1000 cycles. The results show no electro-optical failures. A slight increase in reverse current (IR) was observed. This increase in IR was not a concern as it is within the product specification limit [12]. The results from this earlier work were not a satisfactory as it was not able to correlate the crack severity against the LED's electro-optical properties. Hence the present investigation was carried out. The objective of the present investigation is the same as the previous work. However, the present work uses extreme bond forces to ensure severe cracks at the die substrate are formed that may potentially affect the electro-optical properties of the LEDs.

2 Experimental Methodology

The experimental methodology is illustrated in figure 3. The AlInGaP die samples were taken from electrically characterized wafers. The Ge substrate is a single crystal Ge, having a face-centered-cubic (FCC) diamond lattice with (111) cleavage plane [13]. These dice were serialized on mylar carrier tape for traceability purpose. DA equipment was used to create cracks at the LED substrate. The force acting on the substrate through the ejector pin can be controlled by the DA machine. To ensure that the force acting on substrate is accurate the DA machine has to be set up correctly. Once the DA equipment was set up and the ejector pin and bond head were checked for alignment, the Keyence bond force tester was then installed on the bonder to check the force. Several trials were carried out to check indentation force consistency. Final confirmation of the force consistency was carried out using a hand held bond-force tester - Correx Tension Gauge [14]. This was to confirm the Keyence bond-force tester measured accuracy before starting the experiment.

The experiment was conducted at room temperature. The ejector pin tip was semi-spherical in shape as illustrated in figure 2. This ejector pin was a standard ejector pin supplied for the LED industry by Micro-mechanics [15]. The ejector pin tip radius, R , for this research was 25 μm . This is widely used for small die size at 300 μm by 300 μm .

The experiment commenced with a force of 180 gF and continued with 190gf, 200 gf and 210gf, respectively. At an indentation force greater than 210 gF the dies completely disintegrated, hence it was not possible to proceed further above this force. Each cell consisted of 120 dice. Indented dice were segregated using different Mylar to avoid

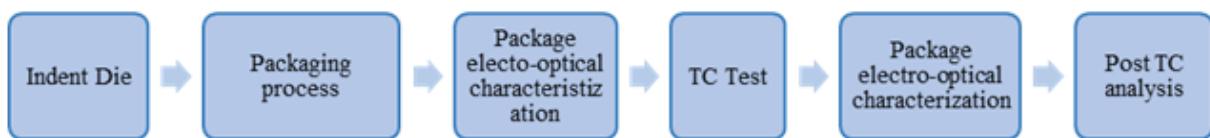


Figure 3: Experimental Procedure.

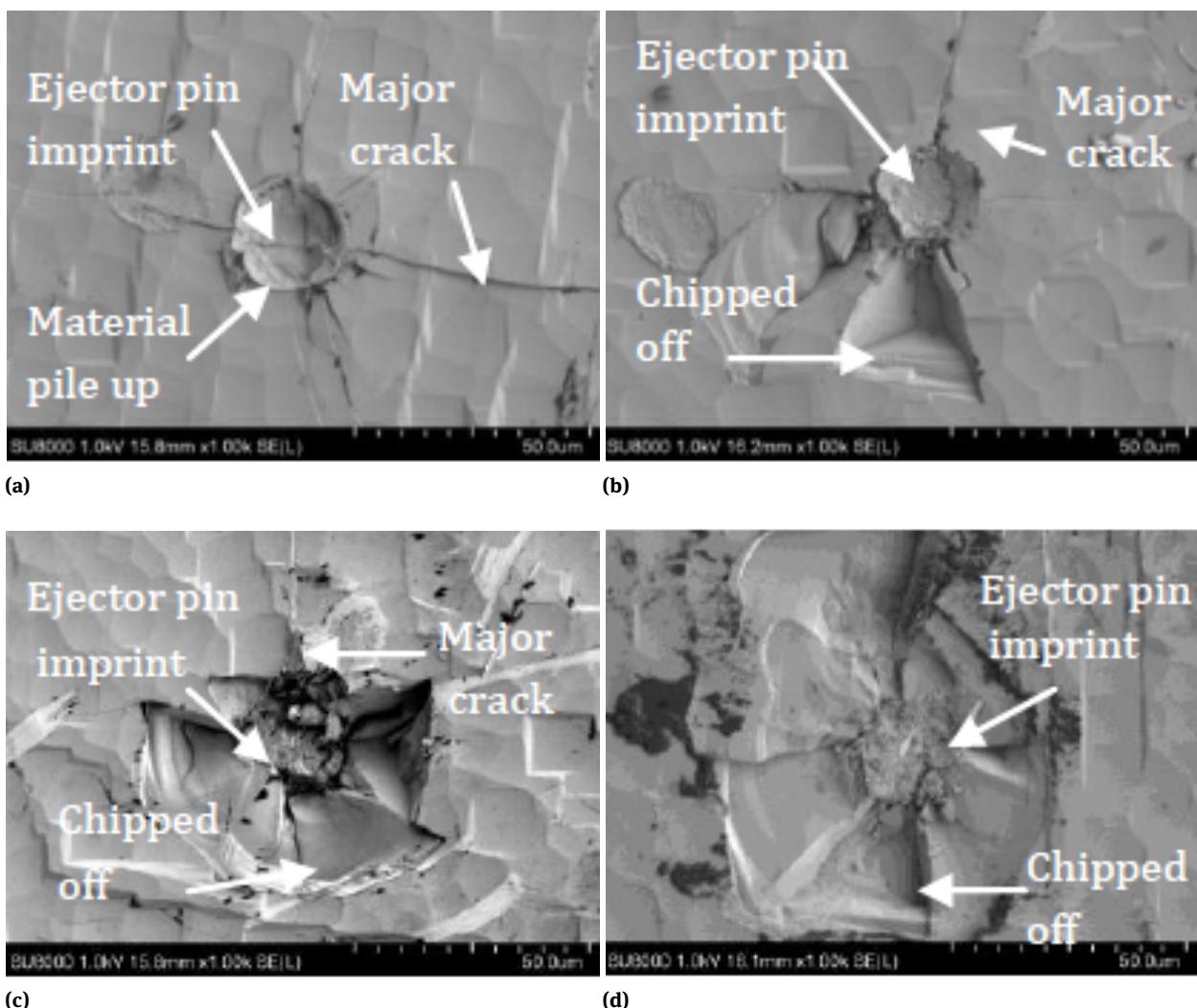


Figure 4: SEM analysis on indented die before TC test, (a) 180gF bond force, (b) 190gF bond force, (c) 200gF bond force, (d) 210gF bond force.

mixing. The indented dice were packaged on a stable LED package and an electro-optical test was performed to segregate good and bad parts. All the cells passed the electrical and optical test with a 100% success rate. These units were mounted on PCB boards and sent for a Temperature Cycle (TC) test in accordance with Jedec standard – JESD22-104D [16]. Here these PCB boards were placed in a TC chamber in a position with respect to the air stream such that there was no obstruction to the flow of air across

and around each PCB. The temperature that the PCB was exposed to was in the range of -40°C to $+100^{\circ}\text{C}$ in a cycle of 15 minutes between each temperature. The electro-optical properties of the LEDs were measured using an Instrument System's Compact Array Spectrometer (CAS) LED tester at certain intervals [17]. After completion of the TC test, several LEDs were electrically analysed using Hewlett Packard (HP) curve tracer. Some LEDs were mechanically

cross-sectioned to check the die crack formation using a Hitachi, Scanning Electron Microscopic (SEM).

3 Results

3.1 Crack Formation Analysis

The SEM results of cracked dies before TC are illustrated in figure 4. At an indentation force of 180 gF, as illustrated in figure 4a, the ejector pin imprint was clearly embedded in the backside of the die (Ge substrate). Major crack-lines were visible even at low magnification scope. Material pile-ups were seen on the surrounding area of the ejector pin mark. At 190 gF, as illustrated in figure 4b, a small chunk of Ge substrate was found to be missing. Major crack-lines and material pile-ups were also visible. The topology of the missing material area is at a certain angle as it follows the diamond lattice structure of Ge (111) cleavage plane. At 200 gF, more material chipped off similar to a half circle shape. The missing material topology at the substrate was fairly similar to that observed in the 190 gF indented die. At 210 gF a lot more material chipped away and formed a circular shape. At any bond force greater than 210 gF, the die totally disintegrated. This Ge substrate could not tolerate forces beyond 210 gF.

3.2 TC test Result and Impact of Cracked Ge substrate to LED electro-optical performance

Many researchers have reported that cracked die degrades the LED electro-optical properties and can cause serious electrical failure [4, 18]. Shalesh *et al.*, [19] explained that even an ordinary LED can fail due to cracks in the active area when subjected to a stress test. It can be clearly seen that stress can cause LED failure. In our previous work we purposely created cracks on the Ge substrate of AlInGap die and stressed them in PCT test. The findings showed no significant impact to the LED electro-optical properties [12]. However, this test did not meet the investigation objective. In this present work we purposely created severe cracks on the Ge substrate of the LED using very high die bond forces and stressed it in TC tests to see the impact on the LED electro-optical performance.

The TC test results of this investigation showed an unexpected result. The electro-optical performance of all the cells remained stable throughout the TC test. No major change was observed after 1000 cycles of the TC test. The

LED forward voltage (Vf) as illustrated in figure 5a and b shows all cells were stable to within a 0.1% difference of measured values at 0 cycle and 1000 cycles TC. The Vf uniformity within the 180 gF and 210 gF cells was on average at 2.113 V with 0.001 V standard-deviation (STD) and 2.115 V with 0.005 STD, respectively. This is perfectly normal and within the product specification and tester measurement tolerance range [20, 21].

The brightness intensity after TC test, as illustrated in figure 5c and 5d, changes less than 1% for all cells. This is also within the testing tolerance of the test equipment [17]. The unit brightness uniformity within the 180 gF and 210 gF cells was on average at 3.142 cd with 0.034 cd STD and 3.113 cd with 0.066 cd STD, respectively. This means the brightness uniformity represent 1.1% and 2.1% respectively. To further understand if this variation was truly impacted by the crack severity, a comparison was made with fresh units that had no cracks. Figure 5e illustrates the brightness of 100 units that had no cracks that came from the same wafer batch that was used for this evaluation. The brightness uniformity within this cell was on average 3.109 cd with 0.056 cd STD, representing 1.80% uniformity. The brightness uniformity of the cell without cracks is in between cells 180 gF and 210 gF.

The other cells (190 gF and 200 gF) showed the same result, they are not elaborated further in this paper.

4 Discussion

4.1 Bond Force and Crack Formation

To understand this cracked die phenomenon, one has to understand the fundamentals of crack formation and the mechanics of the material. Crack formation is due to the fact that stress acting on the atomic bond exceeds the inter-atomic bond strength [22]. High stress is required to break a Ge inter-atomic bond [23]. The stress at which these bonds rupture takes place is also called ideal strength, (δ) and is described in equation (1) [24]:

$$\delta \approx E/15 \quad (1)$$

Here E is the Young Modulus Elasticity of Ge; 103 GPa [13]. The ideal strength of Ge was calculated using equation (1), which was roughly 6.87 GPa, while the stress applied to the Ge substrate through the ejector pin at 180 gF bond force was about 22.5 GPa. This was calculated using equation 2 derived from Hertz contact mechanics [7, 25], where $a = 5 \text{ um}$ (measured value). F is the in-

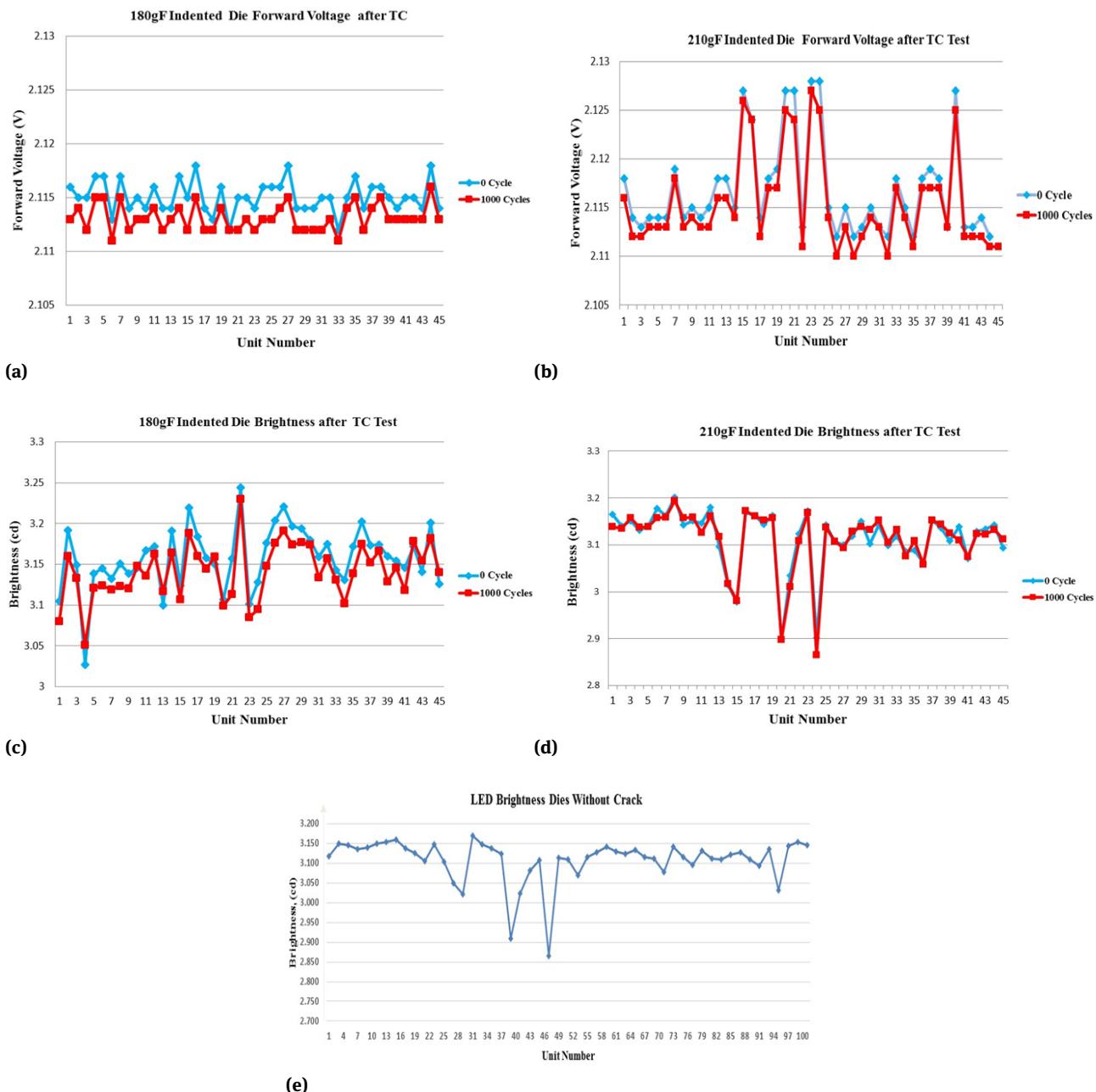


Figure 5: Electro-optical performance of the indented die after TC test, (a) 180gF indented die forward voltage (V) after TC test, (b) 210gF die forward voltage (V) after TC test, (c) 180gF indented die brightness (cd) after TC test, (d) 210gF indented die brightness (cd) after TC test, (e) LED brightness dies without crack before TC test.

indentation force (180 gF).

$$\sigma = F/\pi a^2 \quad (2)$$

a , is the ejector pin spherical surface contact length. Note that a , follows Hertzian contact analysis, and is restricted to condition that the depth of penetration is small relative to the radius of the sphere of the ejector pin tip [23, 25, 26].

By comparing the ideal strength of Ge (6.87 GPa) and the stress induced by the ejector pin at 180 gF (22.5 GPa)

it can clearly be seen why the crack occurs, the ejector pin stress is far greater than the ideal strength of Ge. At 22.5 GPa, stress from the ejector pin overcame the inter-atomic forces in the Ge substrate. Separation occurred when stress applied to the Ge substrate was sufficient to exceed the maximum force per bond. As a result, fracture was bound to occur [27].

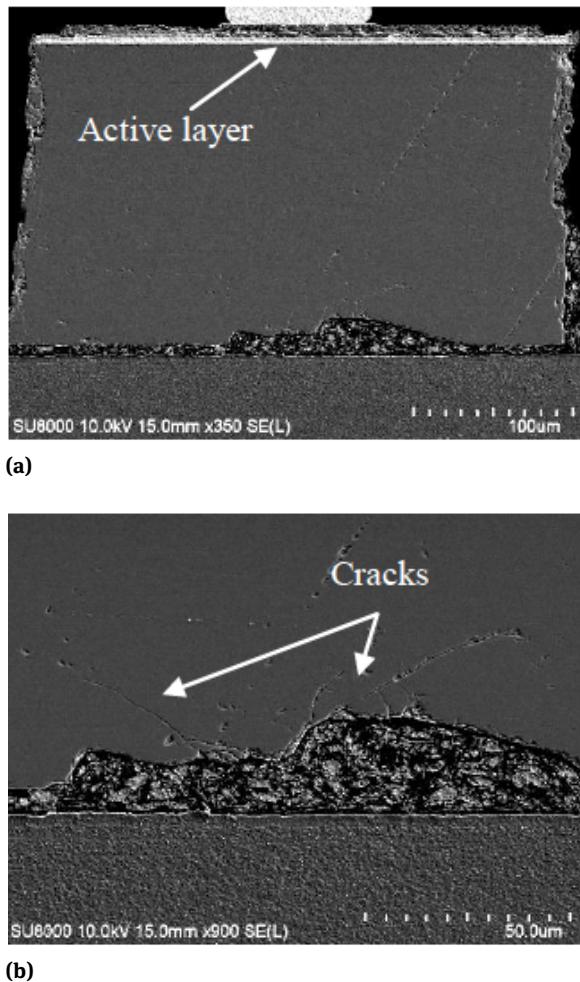


Figure 6: Cross-section view of the units after TC test showing cracks. (a) Cross-section view showing active layer of die and crack formation. (b) Detail view of cracks at the bottom of die substrate.

4.2 Impact of cracked Ge substrate to LED electro-optical performance

The results from the TC test as illustrated in figure 5a to 5d clearly show the cracked die have small changes in V_f and brightness at 0 cycle compared to 1000 cycles. These small changes can be due to the external influences *i.e.* ambient temperature and precise mechanical set-up. They are not a concern as they are within the testing tolerance and product specification [17, 21].

On the other hand, there was some non-uniformity observed in the brightness intensity within the cells. Cells 180 gF and 210 gF have 1.1% uniformity and 2.1% uniformity respectively. The control cell has uniformity at 1.8%. If the control cell already has a uniformity of 1.8% it shows that this variability in uniformity is not a die crack issue but instead could be another issue. One potential reason could be the dice itself. In this investigation the dice were

taken randomly from one wafer and it is well known that the dice within one wafer can have some brightness variation [28]. The center and outer values of wafer brightness intensity are different and can have up to 3.9% variation as reported by Mike Cooke. Hence, it is highly suspected this variation most likely comes from die selection from the wafer and since these dice were not sorted optically this variation is expected.

This result opens up the question as to why these dice were not significantly affected by a cracked substrate. To understand this, the LEDs were mechanically cross-sectioned and analysed using SEM.

The cross-section finding shows as illustrated in figure 6, that the crack at the bottom of the die did not propagate further to the active layer (epitaxial). It is well understood that as long as the active region is not affected, LED performance will not be affected [29–31]. This means, the crack did not propagate further because the stress created by the TC test was lower than the Ideal strength of Ge. The stress the die undergoes during the TC test can be calculated using equation (3), as shown below [9].

$$\sigma = E\alpha(T - T_{ref}) \quad (3)$$

E is the modulus elastic, α is the coefficient of thermal expansion (CTE), T is temperature and T_{ref} is the room temperature.

The dice in these LEDs were glued on the leadframe using a silver filled glue. This glue helps to bind the dice to the leadframe. When the temperature was raised to 100°C, the Ge substrate and glue expanded together. The glue that binds the die, expands more than the Ge substrate because the CTE (α) of the glue is larger than Ge. Hence, this glue gives a certain amount of pull force at the die when the glue expands. When the temperature is below zero, the Ge substrate and glue contract and cause the die to compress. In total, the stress induced by the TC test was the cumulative stress of the Ge and silver glue.

When modulus elastic, E of Ge was 103 GPa [13], CTE, α of Ge is 5.9 ppm [11], modulus elastic E of silver filled glue was 6.4 GPa [32], CTE, α of silver glue was 30 ppm [32], T was 100°C (max TC temperature) and T_{ref} was at 25°C (room temperature), the normal stress induced on the die, σ was 60.0 MPa. The TC temperature and reference temperature was taken from the jedec standard [16]. However, when the T is -40°C (lower limit ambient temperature in the TC test), the CTE (α) of the glue is 30 ppm (below T_g) [32]. Hence, the total compression stress is -52 MPa.

Based on equation (3), the maximum normal stress created by the TC test, σ , is 60.0 MPa, while the ideal strength of the Ge substrate is 6.87 GPa. It is obvious that the Ideal strength of Ge is far greater than the stress created

by the TC test. Hence, the stress from the TC test is not able to further propagate the crack in the severely cracked die. As a result, the cracks did not propagate, the active layer was not affected and the LED performance after the TC test (1000 cycles), remained the same.

4.3 Failure Analysis of Indented Chips before and after TC test

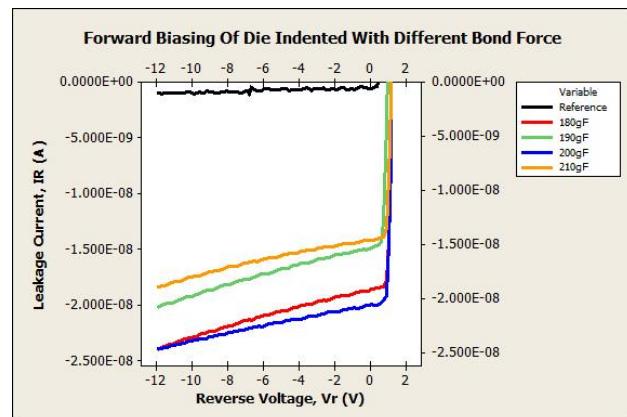
Some of the units from the different bond forces, before and after the TC test, were analyzed using an HP curve tracer for their reverse bias characteristic.

The result clearly shows that in every unit with a cracked die small leakage current was observed compared to the reference unit (without a crack). This could be seen in both units before and after the TC test, as illustrated in figure 7a and 7b.

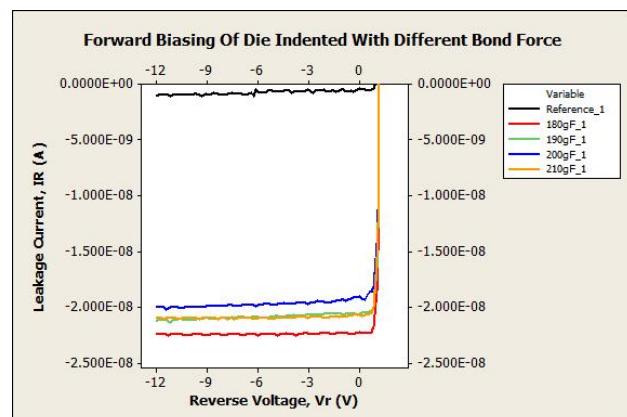
This finding clearly shows that severely cracked dice at the Ge substrate have a small increase in leakage current. Even though the leakage is insignificant compared to product specification it is worth discussing from a technical point of view. The increase in reverse current may have come from a defect on the active layer. The stress induced on the die during the indentation process may have an effect on the active layer that probably causes small defects. A similar phenomena was reported by Wang *et al.* in their investigation on leakage current of an LED [33]. Their finding confirms that damage to an LED increases the number of defects and leads to a leakage current pathway in the active layer. This is quite similar to this current investigation where high stress was induced on the dice. This stress may have caused some damage in the active layer. However, the leakage current increase observed in this present investigation is too small and poses no risk. In fact, it is smaller than the product specification value [20].

5 Conclusion

It can be observed from this present work that severe cracks occurred at the Ge substrate when it was subjected to a bond force of 180 gF and greater. The die substrate can only tolerate a bond force of up to 210 gF as any force greater than 210 gF means that the die is totally disintegrated. These cracked die were subjected to a TC test and the results were rather unexpected as the cells did not degrade at all. Even the worst cracked die showed no electro-optical performance degradation. This result is the same as in our prior work on less severely cracked dice. Due



(a)



(b)

Figure 7: Reverse characteristic of units before and after the TC test. (a) leakage current of die indented with different bond force **before** the TC test. (b) leakage current of die indented with different bond force **after** the TC test.

to the fact that the cross-section of the dice revealed the cracks are still far away from the active layer they do not affect the electro-optical properties of the LED. This investigation certainly proved that the Ge substrate with a lattice (111) cleavage plane was tough. It is able to tolerate the TC stress for up to 1000 cycles and prevented cracks at the bottom of the substrate propagating further. Small current leakage was observed in all the cracked die units compared to the reference units (without cracks). However, the leakage current value was small compared to the specification value and as a result there were no major concerns.

The findings from this investigation certainly challenge the current wisdom that a cracked substrate of an AlInGaP LED is a high risk and may harm LED performance. However, further investigations on tolerance levels beyond a 1000 cycle TC test would yield very valuable information.

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References

- [1] Zukauskas A., Shur M.S., Gaska R., *Introduction to solid-state lighting*, John & sons, Inc., New York, 2002.
- [2] Meneghini A.T.M., Mura G., Meneghesso G., Zanoni E., *A Review on the Physical Mechanisms That Limit the Reliability of GaN-Based LEDs*, *IEEE Transactions on Electron Devices* 57, 2009, 108–110.
- [3] Barton D.L., Osinski M., Perlin P., Eliseev P.G., Lee J., *Single-quantum well InGaN green light emitting diode degradation under high electrical stress*, *Microelectronics Reliability* Elsevier, 39, 1999, 1219–1227.
- [4] Lafont U., van Zeijl H., van der Zwaag S., *Increasing the reliability of solid state lighting systems via self-healing approaches: A review*, *Microelectronics Reliability* Elsevier, 52, 2012, 71–89.
- [5] Chen C.H., Tang J. Y., Tsai W.L. *et al.*, *Determination of LED die strength*, in: *Electronic Materials and Packaging* (19–22 Nov. 2007, Daejeon, S.Korea), IEEE, Daejeon, 2007, 1–6.
- [6] Japan Creation Manufacturer - Full Automated Die Bonder Operation Manual, Tosok Die Bonder, 175, 2010, 1–5 (unpublish data from OSRAM Opto Semiconductors).
- [7] Fisher-Cripps A., *IBIS Handbook Of Nanoindentation Book*, Fisher-Cripps Laboratories Pty. Limited, New South Wales, 2009.
- [8] Chen Z., Zhang Q., Wang K., Luo X., Liu S., *Reliability test and failure analysis of high power LED packages*, *J. of Semiconductors*, 32, 2011, 1–4.
- [9] Fan J., Yung K., Pecht M., *Physics-of-failure-based prognostics and health management for high-power white light-emitting diode lighting*, *Device and Materials Reliability*, *IEEE Transactions*, 11, 2011, 407–416.
- [10] Gao S., Hong J., Shin S., Lee Y., Choi S., Yi S., *Design optimization on the heat transfer and mechanical reliability of high brightness light emitting diodes (HBLED) package*, in: *58th Electronic Components and Technology Conference* (27–30 May 2008, Lake Buena Vista, FL, USA), IEEE, FL, 2008, 798–803.
- [11] Lu G., Yang S., Huang Y., *Analysis on failure modes and mechanisms of LED*, in: *Reliability, maintainability and safety* (20–24 July 2009, Chengdu, China), IEEE, Chengdu, 2009 1237–1241.
- [12] Annanah L., Devarajan M., *Investigation on electro-optical performance of aluminium indium gallium phosphate light emitting diode with cracked substrate*, *Materials Science in Semiconductor Processing*, 36, 2015, 84–91.
- [13] Claeys C., Simoen E., *Germanium-based technologies: from materials to devices*, Elsevier, Oxford, 2011.
- [14] Correx Tension Gauge – Instruction for User, in: www.chescientific.com/ecat/Eng/correx.pdf, 2016.
- [15] Micro Mechanics, Ejector Pin Configuration, in, *Micro Mechanics*, Online, 2016, pp. World Wide Web: <http://www.micro-mechanics.com/product.php?id=102>.
- [16] JEDEC Standard JESD22-A104D, “Temperature Cycling,” © JEDEC Solid State Technology Association, 2009, 2–5.
- [17] Nägele T., Distl R., *Handbook of LED Metrology*, Instrument Systems GmbH, version, Munich, 1999.
- [18] Jiang Y., Song X., Lam T. F., Samatitchon S., *FBGA Die Crack Issue Analysis*, in: *2007 International Symposium on High Density packaging and Microsystem Integration* (26–28 June 2007, Shanghai, China), IEEE, Shanghai, 2007, 1–2.
- [19] Shailesh K., Kurian C. P., Kini S. G., *Solid State Lighting Reliability from Failure Mechanisms Perspective: A Review of Related Literature*, *International J. of Semiconductor Science & Technology*, 2012, 3, 43–50.
- [20] OSRAM Opto Semiconductors Datasheet, LA E67F – Power TOPLED, 2013, 1–10.
- [21] Keithley, *Low Level Measurement Handbook – Precision DC current, Voltage and Resistance Measurement*, Keithley – A Tektronic Company, Cleveland, Ohio, 2013.
- [22] Van Vlack L.H., *Elements of materials science and engineering*, Addison-Wesley Pub. Co., Michigan, 1987.
- [23] Annanah L., Devarajan M., *Analysis of crack formation in germanium substrate at AlInGaP die bonding process*, *International J. of Material Science and Applications*, 4, 2015, 1–6.
- [24] Ashby M.F., Jones D.R., *An Introduction to the Properties and Applications*, Pergamon Press, Oxford, 1980.
- [25] Lawn B.R., *Hertzian Fracture in Single Crystals with the Diamond Structure*, *J. of applied Physics*, 39 1968, 4828–4836.
- [26] Oliver W.C., Pharr G.M., *Measurement of hardness and elastic modulus by instrumented indentation: Advances in understanding and refinements to methodology*, *J. of materials research*, 19, 2004, 3–20.
- [27] Dowling N.E., *Mechanical behavior of materials: engineering methods for deformation, fracture, and fatigue*, Prentice hall, 1993.
- [28] Cooke M., *Azzuro boosts nitride LED on silicon uniformity with strain engineering*, *Semiconductor Today*, 2013.
- [29] Krames M.R., O.B. Shchekin O.B., Mueller-Mach R., Mueller G. O., Zhou L., Harbers G., Crawford M.G., *Status and future of high-power light-emitting diodes for solid-state lighting*, *J. of Display Technology*, 3, 2007, 160–175.
- [30] Nakamura S., *The roles of structural Imperfections in InGaN Based Blue Light Emitting Diodes and Laser Diodes*, *Science*, 281, 1998, 957.
- [31] Schubert F. E., *Light Emitting Diode*, Cambridge University Press, New York, 2006.
- [32] Sumitomo Bakelite Co. Ltd, *Sumiresin Excel CRM 1084F – Electrical conductive die attach paste*, in, 2004, pp. Available from World Wide Web: www.tomore.cn/products/Sumitomo/CRM-1084F.pdf.
- [33] Wang Y., Tseng C., Chen Y., Chen N., *Influence of strong reverse-bias on the leakage behavior of light-emitting diodes*, in: *Conference on Lasers and Electro-Optics/Pacific Rim* (26th August 2007, Seoul, S.Korea), Optical Society of America, Seoul, 2007, 1–2.