#### Review

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# Optimization of non-linear conductance modulation based on metal oxide memristors

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Abstract: As memristor-simulating synaptic devices have become available in recent years, the optimization on non-linearity degree (NL, related to adjacent conductance values) is unignorable in the promotion of the learning accuracy of systems. Importantly, based on the theoretical support of the Mott theory and the three partial differential equations, and the model of conductive filaments (CFs), we analyzed and summarized the optimization schemes on the physical structure and the extra stimulus signal from the internal factor and external influence, two aspects, respectively. It is worth noting that we divided the extra stimulus signals into two categories, the combined pulse signal and the feedback pulse signal. The former has an internal logical optimized phenomenon, and the composition of only two parts in each cycle leads to a simple peripheral circuit. The latter can obtain an almost linear NL curve in software stimulation because of its feature in real-time adjustment of signals, but it is complex in hardware implementation. In consideration of space and energy consumption, achieving memristor with different resistive switching (RS) layers can be another optimization scheme. Special attention should be paid to the weaker NL, which could improve learning accuracy at the system level only when the value of other non-ideal properties such as the on/off ratio is within a certain range.

**Keywords:** conductance modulation; memristor; neuromorphic system; non-linearity.

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#### 1 Introduction

The memristor is widely viewed as a potential device in neuromorphic systems as its analog resistive switching (RS) process is suitable to simulate the weight update of a biological synapse (bio-synapse), after showing its developing advantage in recognizing the digital state of storage [1-4] and analog states of computational fields [5-10]. Nearly a decade of research has reinforced the realizability of memristors in this application area. In these neural morphic applications, the memristor needs to exhibit an analog RS behavior (having multi-resistance states) rather than binary resistance states, and some of its non-ideal properties lead to a negative influence on the learning accuracy of the neuromorphic system [11–13]. The focus of this review is on the performance optimization of a memristor, and the optimization object is the non-ideal characteristic of the conductance modulation of the memristor. The key sections of the review are Sections 2 and 3, which discuss the theory and mechanism of supporting the optimization object and the feasible schemes from the external conditions to achieve optimization, respectively.

To make a clear comparison between the memristor and the bio-synapse, a model diagram of these two concepts is shown in Figure 1. The weight update of the bio-synapse is the basis for transmitting and processing information [14–16], and the continuous conductivity state switching of memristors can mimic this function of a bio-synapse by enabling the distribution of multiple conductance states [17-21]. So a common concept, non-linearity (NL for short) of the state distribution, becomes the key point. Within this article, all of the non-linear terms we are talking about refer to NL in conductance modulation of a memristor, also known as the NL in the weight update of a synaptic device. A memristor with an ideal NL (=0) can simplify the weight update process and hardware circuit, and improve the learning accuracy [22] in a neuromorphic system. The most intuitive expression of the device with a higher NL (close to 1) is the phenomenon of two stages in conductance modulation curves [23–28], and

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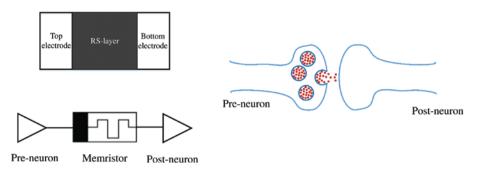


Figure 1: Comparison between the bio-synapses and the artificial synapses (memristors).

a detailed explanation of NL is given in the second part of this article.

Metal oxide memristors usually have a typical metalinsulator-metal (MIM) structure, and its insulator layer (also known as the RS layer) is made by binary metal oxides (e.g. TiO, [28–31], WO, [32, 33], TaO, [34–42], HfO, [43–47], etc.), perovskite metal oxides [48, 49], chalcogenes [50, 51], and others. Although the RS mechanism of a memristor does not have a unified conclusion so far, the conductive filament (CF) model based on ion/vacancies migration in many research conclusions can give a good degree of coverage of the corresponding experimental data. For example, Shigeoka et al. [52] showed the work on a memristor based on Ta<sub>2</sub>O<sub>5</sub> by using the CF model. Bousoulas et al. [53] demonstrated its research on Ti/TiO2 -based memory devices based on the CF mechanism. Qu et al. [33] demonstrated the reason for the existence of CFs using the experimental results of a WO based memristor. In addition, migration of ions/vacancies in the RS layer is thought to be associated with NL [5, 37–39, 54, 55], and further calculations of particle migration provide theoretical support using the Mott theory and the finite element method (FEM) [56-58]. The Mott theory was the cornerstone of research related to particle migration. The FEM uses the mathematical method to simulate the real physical system and is used as the model basis for the internal state analysis of memristors. Kim et al. [59–63] used this model in a series of research related to memristors in recent years. Based on these theories, scientists focused much of their attention on the optimization scheme of NL based on the ion transport of an RS material, such as doping and the multi RS layer [64, 65].

For other optimization schemes of NL, using smarter stimulus signals are suggested, which looks for a series of signals that balances the device between NL and feasibility. In this review, Section 2 is about NL optimization in a simple one-dimensional (1D) rigid point ion model

proposed by Mott and Gurney [66], which results in a self-consistent solution of three partial differential equations (PDEs). Two kinds of NL optimization schemes, the smarter stimulus signal and the multi RS layer, are stated in Sections 3 and 4, respectively. In Section 5, we summarize the optimization schemes, from the four aspects of NL optimization, feasibility, novelty degree, and consumption. In Section 6, we summarize the direct and indirect effects of NL change on learning accuracy in a neuromorphic system.

## 2 Causes of the two-stage phenomenon

#### 2.1 The two-stage phenomenon

The I-V curve cluster is the most common form of graphic used in characterizing a multi-state modulation of a memristor, which is taken by applying voltage sweeps with a certain value of the termination voltage ( $V_{\rm stop}$ ) or a certain value of the complaint current ( $I_{\rm cc}$ ). The I-V curves are the basic characterization method in the field of memristor research. At the same time, in order to study the analog RS behavior of the memristor, especially its linearity of the conductance modulation, the characteristic curve that indicates the conductance to change with the increase in the external stimulus loading time becomes the main means, as shown in Figure 2.

Figure 2A shows the corresponding experimental results of the I-V relationship based on the TE/HfO<sub>x</sub>/AlO<sub>x</sub>/BE memristor device, by Kim et al. [59]. In order to obtain more intuitive expression of conductance distribution, the conductance-cycle number (or time) curves are necessary. A high-degree fitting results of the experiment is introduced here to prove the phenomenon of segmentation (Figure 2C), by Wang et al. [67], by applying a pulse sequence with a

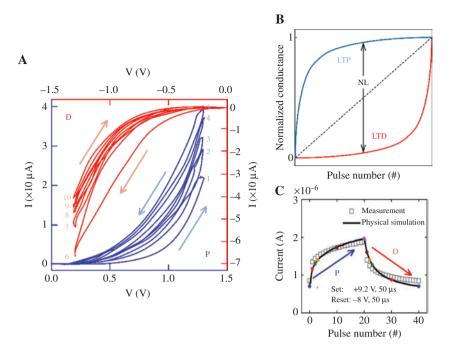


Figure 2: Multi-level RS behavior and the two-stage phenomenon in conductance modulation in the memristor. (A) Multi-level resistive switching properties of the Pd/WO<sub>3</sub>/W device obtained by applying DC sweeps. The number in this figure indicates the sweep sequence. Blue, the set process; red, the reset process. Adapted with permission from Ref. [25]. Copyright 2011 Applied Physics A Materials Science and Processing. (B) Non-linear conductance modulation curve with ideal symmetric P/D curves and normalized conductance as the Y-axis. (C) Ta/ TaO /TiO./Ti device. Non-linear conductance modulation curve obtained by applying AC pulses successively. The hollow point is experimental data, and the black solid curve is the simulation results. Adapted with permission from Ref. [67]. Copyright 2015 Scientific Reports.

constant value in amplitude and frequency (called identical pulse), based on the Ta/TaO\_/TiO\_/Ti memristor.

Figure 3 lists several conductance modulation curves for a memristor with different materials or structures. Not only is this found in the usual two-terminal memristor, a similar phenomenon also occurs in the threeterminal memory transistors [61, 63, 71-78]. Zhu et al., from Beijing University, developed the WSe,-based synaptic transistors. This device shows good performance, especially in terms of conductivity modulation linearity and low energy consumption [61]. In this work, there are no obvious two-stage phenomena in the conductance modulation curve, and the ultralow energy consumption of ≈30 fJ per spike is achieved. The conductance modulation curves show different forms, especially in the aspect of the slope. Based on these results, it can be concluded that the slope of the curve shows a segmentation phenomenon. The segmentation of the slope of the curve in conductance modulation curves of a memristor device is not a special case, but occurs in the vast majority of experiments. Das et al. [79] found the segmentation phenomenon at the Y<sub>2</sub>O<sub>3</sub>-based memristor. Banerjee et al. [80] found this phenomenon for the TiO<sub>2</sub>/Al<sub>2</sub>O<sub>2</sub>-based memristor. Guangyang et al. [72] found this phenomenon at the SnO<sub>3</sub>-based memristor. The segmentation

phenomenon is described as a two-stage phenomenon here in the aspect of the metal oxide memristor.

For a two-stage phenomenon, the slope of the curve is usually segmented to a clear two stages, as the initial stage is significantly higher than the tail, as shown in Figure 2C. In detail, the abrupt change in the adjacent conductance value( $\Delta G$ ) occurs in the first stage, and the gentle change reaches the saturation conductance value  $(G_{max})$  in the second stage. Either memristors exhibit a continuous increase or a continuous decrease in conductance value upon a stimulation pulse with an opposite polarity, corresponding to the characteristics of biosynapses, and these two behaviors can be called longterm potentiation (LTP) and long-term depression (LTD), respectively [81–84]. In order for this phenomenon to be effectively analyzed, the concept of NL proposed by Wang et al. in 2016 [85] was adopted.

$$NL = Max |G_{ITP}(n) - G_{ITD}(n)|, n = 1, 2, 3, \dots, N$$
 (1)

Eq. (1):  $G_{LTP}(n)$  and  $G_{LTD}(n)$  are the conductance values after the nth LTP-pulse and LTD-pulse, respectively. N is the number of LTP-pulse/LTD-pulse.

This concept is based on the image representation shown in Figure 2B, in which the LTP and LTD are

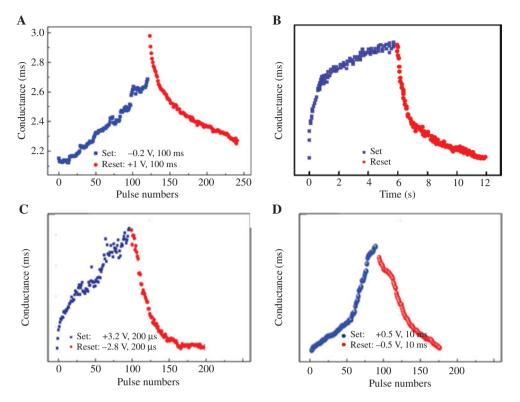


Figure 3: Non-linear conductance modulation curves. (A) Pt/HfO<sub>x</sub>/ZnO<sub>x</sub>/TiN memristor device. Adapted with permission from Ref. [68]. Copyright 2017 Nanoscale Research Letters. (B) TiN/TaO<sub>x</sub>/Pt memristor device. Adapted with permission from Ref. [69]. Copyright 2016 Nanoscale. (C) Pt/TiN/PCMO/Pt memristor device. Adapted with permission from Ref. [26]. Copyright 2010 Nano Letters. (D) Ta/ethyl viologen diperchlorate [EV(ClO<sub>x</sub>)<sub>2</sub>]/triphenylamine-based polyimide (TPA-PI)/Pt memristor device. Adapted with permission from Ref. [70]. Copyright 2016 Journal of Materials Chemistry C.

symmetrically characterized in one dialog, for facilitating the conformance of NL, and NL is defined as Eq. (1).

#### 2.2 Theoretical basis

As a key research direction of memristors in the aspect of internal mechanism, particle migration has been continuously appearing in related research papers. This foundation provides theoretical support for other optimization work. Kim et al. [57, 59], Prezioso et al. [29, 86–88], and Matveyev et al. [10, 89-91] used this as a support to propose NL optimization. Sung et al. [92] worked on optimization on the I-V linearity. Garbin et al. [93] worked on optimization on variability. It is worth mentioning that Mott first proposed the theory of particle migration in 1948 [94], called the Mott theory, shown as Eqs. (2) and (3), to describe particle migration. Here, a is the effective escape distances, and  $E_a$  is the activation energy for the hopping process, and they are all determined by the kind of particle and the kind of material in which the particles migrate.

$$D = \frac{1}{2}a^{2}f \exp\left(-\frac{E_{a}}{kT}\right), D_{0} = \frac{1}{2}a^{2}f$$
 (2)

$$v = af \exp\left(-\frac{E_a}{kT}\right) \sinh\left(\frac{aqE}{kT}\right)$$
 (3)

Eqs. (2) and (3): D is the ion diffusivity, f is the attempt-to-escape frequency,  $E_a$  is the activation energy for the hopping process, a is the effective hopping distance, T is the local temperature, E is the local electric field, v is the drift velocity, k is the Boltzmann constant, and q is the charge quantity.

Larentis et al. [95] used three partial differential equations to establish a physical model of a memristor driven by particle migration in their paper in 2012. In recent research, this method was followed and optimized by other researchers. In 2014, Kim et al. [60] proved this method by comparing the experimental data from a  $\text{TaO}_x$ -based memristor. After that, they divided the internal state variables w (used to describe the size-doped area) into g (length of CFs) and r (radius of CFs) because of the appearance of

the CFs model. This work led researchers to analyze memristors using second-order or even higher-order models. Dipesh et al. [96] made the numerical modeling as the theoretical basis of heat transfer. Sadi et al. [97] made this theory the simulation methodology in their work based on SiO... For exploring the resistive switching mechanism of a memristor, it is necessary to investigate the activity track and law of carriers in the memristor device bulk. Thus, the simulation of the RS process requires the PDEs: (1) a drift/diffusion continuity equation for V<sub>0</sub> transport, (2) a current continuity equation for electrical conduction, and (3) a Fourier equation for Joule heating, as shown in Eqs. (4-6).

V transport

$$\frac{\partial n_{_{D}}}{\partial t} = \nabla \cdot (D\nabla n_{_{D}} - vn_{_{D}} + DSn_{_{D}}\nabla T) \tag{4}$$

**Current continuity** 

$$\nabla \cdot \sigma \nabla \Psi = 0 \tag{5}$$

Joule heating

$$\mu C_{p} \frac{\partial T}{\partial t} - \nabla \cdot \kappa_{th} \nabla T = \gamma \cdot \sigma |\nabla \Psi|^{2}$$
(6)

Eqs. (4–6):  $n_p$  is the concentration of  $V_0$ ,  $\psi$  is the potential, and *T* is the temperature.

A simulation of this theory can be achieved through the establishment of an effective model based on the finite element method (FEM), in which the value of  $n_n$ ,  $\psi$ , and T can be calculated within a numerical solver. The establishment of the model requires a one-to-one correspondence with the structure of the memristor. In particular, the multi-layer RS layers of different materials cannot be mixed together for discussion. In order to facilitate the explanation of this theory, the CF model of a memristor with a simple structure based on FEM is given here (Figure 4A, B). All of the meanings and units of the variables or constants, involved in the Mott theory and the three PDEs, are summarized in Table 1.

Ion migration is described by a flux in units (cm<sup>-2</sup> s<sup>-1</sup>), including diffusion  $(j_{\text{diff}})$  and drift  $(j_{\text{driff}})$  [57, 95] components, as the Mott theory elaborates. Both these two processes rely on ion hopping. External electric field stimulation will change the difficulty of particle migration. Specifically, in the direction of the electric field, the barrier of particle migration decreases, and particles migrate easier toward the same direction. On the contrary, particle migration becomes more difficult in the opposite direction of the external electric field. This process results in a directional ion drift (Figure 4C). On the other hand, the diffusion process

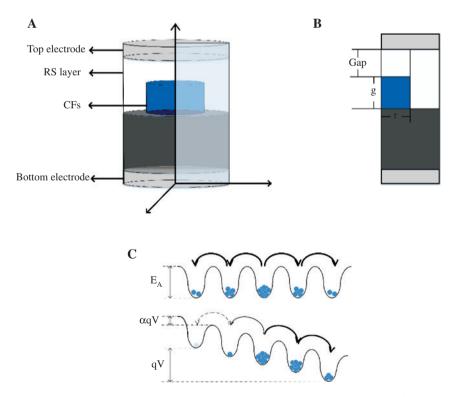


Figure 4: Model of memristor based on the FEM and the particle transition model. (A) 3D CF model of a memristor with a simple structure based on FEM. (B) 2D CF model of a memristor. (C) Particle transition model.

**Table 1:** The detailed information of the three PDE-related parameters.

Char.	Unit	Meaning			
Parame	eters in consta	nts			
а	Nm	Hopping distance			
$E_{a}$	eV	Ion migration energy barrier			
f	Hz	Escape attempt frequency			
γ	_	$\gamma$ = 1 for DC			
		$\gamma = 2$ for AC			
Parame	eters from mea	surements and assumption			
g	Nm	Length of the CF			
r	Nm	Radius of the CF			
$r_{_m}$	nm				
$\rho$	S/cm	Resistivity of the CF			
$\sigma$	$\Omega^{-1}$ cm $^{-1}$	Electrical conductivity			
$\sigma_{_{0}}$	$\Omega^{-1}$ cm $^{-1}$	Electrical conductivity pre-exponential factor			
$E_{AC}$	eV	Activation energy for conduction			
	lent variables				
$n_{p}$	cm <sup>-3</sup>	Concentration of V <sub>o</sub>			
T	K	Temperature			
$\psi$	V	Potential			
Parame	ters about par	rticle migration			
V	cm s <sup>-1</sup>	Drift velocity			
D	$cm^2 s^{-1}$	Diffusivity			
S	$K^{-1}$	Soret diffusion coefficient			
Flux					
$D\nabla n_{D}$		Fick diffusion flux			
$V n_D^{\sigma}$		Fick drift flux			
DSn	$_{0}\nabla T$	Soret diffusion flux			
Parame	ters for currer	nt			
10	Α	_			
$V_{0}$	V				
$g_{m}^{\circ}$	nm				
	ters determin	ed by materials			
$\mu$	kg/cm³	Ion mobility			
$C_{p}$	$J~K^{-1}~cm^{-3}$	Heat capacitance			
$k_{th}^{r}$	$W\ cm^{\scriptscriptstyle -1}\ k^{\scriptscriptstyle -1}$	Thermal conductance			
$\delta^{''}$	_	Heat dissipation factor			
Н	_	Temporal heat factor			

of ions depends on both the temperature gradient and the carrier concentration gradient. Therefore, calculating the carrier concentration distribution in the device bulk is of great significance for investigating the RS mechanism of it.

To solve the three PDEs, boundary conditions of  $\psi$  and an approximately maximum carrier density are needed, as shown in Table 1. A model for electrical conductivity in the RS layer and in CFs is considered to be thermally activated, as shown in Table 1.When making calculations, the researchers assume that  $\sigma_0$ ,  $E_{AC}$ , and  $k_{th}$  are linearly related to  $n_D$ , and the relevant starting and ending values are related to the material of the RS layer. It must be said that such assumptions have been verified [56, 58, 95] as not affecting the validity of the calculations. In the early simulations, the factor of temperature in the memristor

device bulk was generally ignored. The specific operation was to set the device bulk temperature equal to room temperature ( $T_{\rm o}$ ), and regard the heat transfer or divergence. It has been verified [57, 98] that such assumptions lead to large differences between the calculated and experimental results. The Joule heating [62, 99–102], caused by CF connectivity in the device, causes a significant temperature change in the device when it is in the RS process, affecting particle diffusion process, so as for the conductivity of the device.

#### 2.3 Particle migration in two stages

From the perspective of the CF morphological changes in the memristor alone, conclusions that are consistent with the three PDEs simulation results can be obtained. Alessandro et al. [103] used the CF model to be the explanation of their experimental results. Lu et al. [104] made their research based on the CF model and showed the twostage phenomena in the forming process of the CFs. Zhu et al. [65] used simulated 2D maps to indicate the oxygen vacancy (V<sub>o</sub>) concentration distributions in a memristor, in which there is significant expanded phenomena in the horizontal direction about the CFs. In order to more intuitively demonstrate the impact of particle migration on the RS behavior, we summarized and made a diagram of it shown in Figure 5. V<sub>o</sub>s are present as doping in PDE simulation and are considered as constituent substances of the CFs. Similarly, the continuation of the conclusion by Gao et al. [24, 105] in this subsection places the V<sub>o</sub>s as the main object. It acts as a carrier in the memristor device bulk, and there is migration within the device so that the device can complete the RS process.

The reason for the two-stage phenomenon discussed in this review is analyzed with the features of the conductance modulation curves. The model shown in Figure 5 shows the direction of the CF growth in the memristor device and the effects of the migration of the Vos in different stages of stimulation. The memristor is initially in an off state, which means a high resistance state (HRS), and there are no CFs in the body. Forming process promotes the formation of CFs by applying external stimuli in the form of voltage that is slightly higher than the RS voltage. At the end of this process, which is to remove the voltage stimulus, there are incomplete CFs formed in the memristor device. At this moment, the device is in the HRS state, and a gap [106–109] exists inside it. By applying external stimuli to the device, the gap will be filled with Vos, and the CFs grow to connect the cathode and anode eventually, which is called the set process. At this moment, the

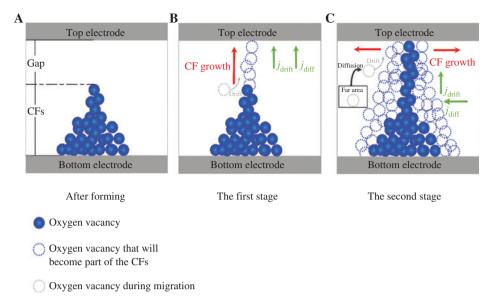


Figure 5: V migration model in a two-stage process in conductance modulation of a memristor. (A) Initial state of the memristor based on the CF model. (B) Model of processes that dominate Vo migration in the first stage. (C) Model of processes that dominate Vo migration in the second stage.

device is in the low-resistance state (LRS). Conversely, when voltage stimulus with opposite polarity is provided in the on state, the V<sub>o</sub>s migrate in the opposite direction. The CFs break after this processing, and the device returns to the off state with incomplete CFs, which is called the reset process.

In the set process, the morphological changes of CFs have different trends with the increase in stimulus loading time. The memristor device is in the first stage at the beginning, when the identical pulse is applied to it. Before the CFs are complete, there is a high electric field in the gap area, and the  $V_0$  (or ion) transmission will be controlled by the drift process, which is driven by an electric field effect, along the V<sub>0</sub> concentration gradient. The main change in the CFs is their length [110], as shown in Figure 5B, which leads to rapid increase in the conductance of the device so that the conductance modulation curve shows a higher slope and the conductance state distribution is sparse. Another important feature in the first stage is that although the conductance value of the memristor can achieve a substantial increase within a smaller number of pulses, it is unsaturated. The reason is that V<sub>s</sub>s in the area near the CFs step into the reduction reaction in the first stage [60], and V<sub>o</sub>s in the area farther away from the CFs need to migrate for a long distance before it, which happens in the second stage. In the first stage, there is just part of the Vos that can participate in the formation of the CFs, and the CFs are not strong enough. When the curve steps into the second stage, the CFs become complete, and the device tends to be metalized. The complete CFs resulted in the reduction of the local electric field, which results in the suppression of the drift process, through the Mott theory shown in Eqs. (2) and (3).

In the second stage, there are obvious differences in the internal changes of the device from the first stage, which must be paid attention to. Several studies simulated the temperature changes inside the device during the RS process and obtained the temperature distribution results with a consistent trend - the areas near the CFs have a higher temperature. Kim et al., from the University of Michigan, worked in this area [56]. Larentis et al., from the University of Texas, did relevant work [95]. Jeong et al. did this work in 2015, and here, we quote their work as shown in Figure 6 [104]. The Joule heating caused by the

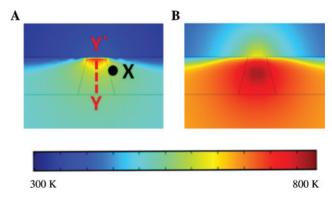


Figure 6: Simulated temperature distribution in the Pd/Ta<sub>2</sub>O<sub>(S-2)</sub>/TaOy/ Pd device at different points. Reprinted with permission from Ref. [104]. Copyright 2015 Applied Physics Letters. (A) Point during the first stage. (B) Point during the first stage.

connected CFs results in a significant temperature gradient that leads to an increased local temperature, as shown in Figure 6. Therefore, the particle diffusion process was enhanced in the second stage, so the CFs can expand in the horizontal direction. Especially, this partial migration process is dominated by the temperature gradient rather than the concentration gradient. In detail, the local temperature of the area where the CFs are located is higher than those of the other areas, which leads to particles migrating toward the CFs. This process can be named as the thermophoresis process as a result of the temperature gradient. The diffusion of the Vos promotes the expansion of the CFs in the horizontal direction [56, 72, 98, 111], which leads to stronger CFs. The reason for the saturated state in this stage is that the V<sub>o</sub>s inside the device bulk that can reach the area where the CFs are located are gradually depleted. Therefore, at the end of the set process, conductance is saturated, and there is no more significant increase when the Vos in the area, even if far away from the CFs, is exhausted.

### 3 The smarter stimulus signal

Spikes were the first to be chosen as a signal source in the memristor stimulus that exists to mimic the type of stimulus signal that a bio-synapse accepts [87, 100, 112, 113]. The device can exhibit LTP and LTD features similar to bio-synapses under continuous spiking stimulation. In addition, stimulated by paired spikes, the memristor device can also achieve the paired-pulse facilitation (PPF) [72], that is, the paired signal is processed by the device to show that the state of the second signal amplitude is greater than the first one. In recent years, in order to simplify the peripheral signal generator circuit, the rectangular pulse signal source is used in the simulation of research about the analog memristor device [114–118]. The amplitude of the pulse signal determines whether the device can achieve RS or not and the value of  $\Delta G$  in the RS process. The frequency of the pulse signal determines whether the conductance value caused by the previous pulse can be maintained until the next pulse arrives at the device.

#### 3.1 Identical pulse

In the simplest form, a pulse sequence with a constant amplitude and frequency, here called the identical pulse, is used as a signal source for stimulating the device (Figure 7A), which is also the signal form commonly used in research in recent years. Stimulated by this signal source, the device generally shows segmented phenomenon in the distribution of conductance value. We collected research data related to an analog RS behavior in the field of memristors in recent years and summarized the experimental results based on the identical pulse, as shown in Table 2. The data in the table shows that the material

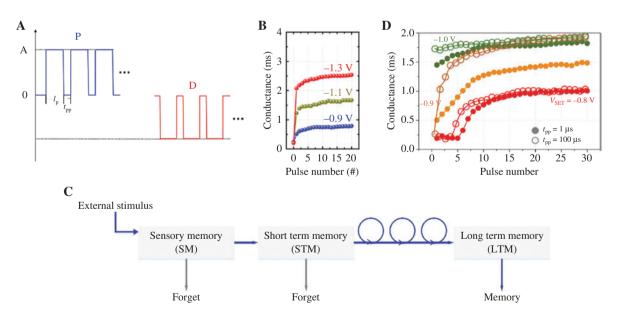


Figure 7: Identical pulse and the response of the memristor to the pulse. (A) Identical pulse. (B) Conductance modulation curves of the programming pulse with different amplitudes based on the Pd/ $Ta_2O_{(S-N)}/TaO_{\gamma}/Pd$  memristor device. Adapted with permission from Ref. [104]. Copyright 2015 Applied Physics Letters. (C) Multiple memory model. (D) Conductance modulation curves of the programming pulse with different amplitudes and  $t_{ro}$  based on the  $Ta_2O_{(S-N)}$ -based memristor device. Adapted with permission from Ref. [98]. Copyright 2015 Nano letters.

**Table 2:** Summary of response of conductivity distribution to identical pulse scheme in memristor devices.

Materials			Programming pulse			Nc (#)	$\Delta G_{ ext{total}}$	Ref.	Year
RS layer	TE	BE	A (V)	Width	N (#)				
Ta <sub>2</sub> O <sub>5-x</sub> /TaO <sub>y</sub>	Pd	Pd	-0.9 1.1	100 μs 10 μs	150	≤25 -	~0.2 mS ~0.2 mS	[60]	2014
$\operatorname{Si}_{2.7\%}$ : $\operatorname{Ta}_{2}\operatorname{O}_{5-x}/\operatorname{Ta}\operatorname{O}_{y}$			-0.9 1.1	100 μs 10 μs		≤25 -	~0.3 mS ~0.7 mS		
$Si_{4.2\%}$ : $Ta_2O_{5-x}/TaO_y$			-0.9 1.1	100 μs 10 μs		≤25 -	~0.5 mS ~0.5 mS		
Ta <sub>2</sub> O <sub>5-x</sub> /TaO <sub>y</sub>	Pd	Pd	-1 -0.9 -1.3	100 ns	20	≤5	~1.5 mS ~1 mS ~2.5 mS	[90]	2015
TaO <sub>x</sub> /TiO <sub>2</sub>	Та	Ті	8.7 -7 -10 9.5 9.2 -8	50 μs	20	≤10	~90 nS ~130 nS ~120 nS ~130 nS ~120 nS ~130 nS	[67]	2015
TaO <sub>x</sub> /TiO <sub>2</sub>	Та	Ti	3 3 -3	5 ms	70 50 50	≤10	~60 nS ~50 nS ~50 nS	[86]	2016
$Ta_2O_{5-x}/TaO_y$	Pt	Pt	0.9	5 μs	100	≤25	~0.4 mS	[65]	2017
TiO <sub>2</sub> :Ag	Ag	Pt	0.4 0.6 0.8	200 ns 300 ns 500 ns 200 ns	30	≤20 ≤16 ≤8 ≤15 ≤5	~0.8 mS ~1.8 mS ~3.8 mS ~3.9 mS ~4.0 mS	[119]	2018
HfO <sub>2</sub>	TiN	TiN	1.5 1.2 -2	10 μs	300	≤25 ≤50 ≤25	~0.4 mS ~0.15 mS ~0.85 mS	[89]	2015
HfO <sub>2</sub>	TiN	TiN	0.85 1 1.2 -1.2 -1.6	1.5 μs	150	- ≤25 ≤10 - ≤50	0 ~20 μS ~90 μS 0 ~80 μS	[90]	2015
HfO <sub>2</sub>	Ti/TiN	TiN	0.8 0.8 -1 -1.1 0.9	100 ms 1 μs 1 μs 1 μs 10 ms	100	≤10 ≤10 - ≤50 ≤20	~200 μS ~50 μS ~50 μS ~150 μS ~50 μS	[120]	2016
HfO <sub>x</sub> /HfO <sub>2</sub>	Ti	TiN	0.8 -1.1 -1	10 μs 100 ms 1 μs 1 μs	100	≤10 ≤10 ≤25 -	~20 μS ~200 μS ~175 μS ~50 μS	[121]	2016
$HfO_x/ZnO_x$	Pt	TiN	-0.2 1	100 ms 100 ms	125	${\displaystyle \mathop{\uparrow}_{\downarrow}}$	~0.4 mS ~0.6 mS	[68]	2017
${\rm Nb_2O_5}$	Al	Al	1.5	10 μs	100	≤10	~90 mS	[122]	2014
$WO_x$	W	Pd	3	400 μs	50	≤10	${\sim}20~\mu\text{S}$	[123]	2014
ZnO	Ti	Pt	5	180 ms	60	$\uparrow$	~5 mS	[124]	2016

Table 2 (continued)

Materials	Programming pulse			Nc (#)	$\Delta G_{ m total}$	Ref.	Year		
RS layer	TE	BE	A (V)	Width	N (#)				
TiO <sub>x</sub>	Pt	TiN	3 2.5 -3 -2.5	1 ms	100	≤40 - ≤20 ≤40	~600 nS ~200 nS ~600 nS ~400 nS	[125]	2016
FeO <sub>x</sub>	Pt	Pt	1.6 1.5 1.45 1.3	100 μs 10 μs 1μs 10 μs	50 50	≤10 ≤5 ≤10 ≤10 ≤20	~0.4 mS ~0.3 mS ~0.2 mS ~0.2 mS ~0.1 mS	[126]	2016
Y <sub>2</sub> O <sub>3</sub>	Al	n-Si	2 2 2.5	50 ms 100 ms 100 ms	100	≤10 ≤10 ≤40	~10 μS ~15 μS ~830 μS	[79]	2018
PEDOT:PSS	Ag	Ta	2	50 ms	50	$\uparrow$	~600 mS	[127]	2013
РСМО	Al		1 2 -2.5 -4	1 ms	100	≤10	~9 nS ~5 nS ~0.4 nS ~100 nS	[22]	2013
PCMO	Pt/TiN	Pt	3 -3	1 ms 100 ms 1 ms 100 ms	100	≤25 ≤25 ≤25 ≤25	~80 nS ~100 nS ~120 nS ~1 mS	[128]	2014
EV(ClO <sub>4</sub> ) <sub>2</sub> + PEO/TPy-Fe	Та	ITO	3 -2	10 ms	50	$\uparrow \\ \downarrow$	~1.5 nS ~0.75 nS	[129]	2016
EV(ClO <sub>4</sub> ) <sub>2</sub> /TPA-PI	Та	Pt	0.5 -0.5	10 ms	90	$\uparrow \\ \downarrow$	~6 mS ~6 mS	[70]	2016
AgInSbTe	Та	Ag	0.6 -0.6	5 μs	50	≤10 ≤10	~8 mS ~8 mS	[130]	2017
Lignin	Au	ITO	0.7 -0.7	100 ms	50	≤20 ≤20	~30 μS ~30 μS	[131]	2017

<sup>-,</sup> there is no obvious two-stage phenomenon;  $\uparrow\downarrow$ , apparent linearity; A, the pulse amplitude; N, the total number of the programming pulse; Nc, the pulse number at the critical point;  $\Delta G_{min}$ , the difference between the maximum conductance and the minimum conductance.

composition of the memristor and the amplitude and the width of the identical pulse signal all have an effect on the experimental data. Based on the data in Table 2, we determine the factors that influence the optimization of NL in the composition of the external stimulus signal and the material composition of the memristor.

An obvious conclusion can be drawn from Table 2 that most binary metal oxide-based memristors have a two-stage phenomenon of conductance modulation. From the aspect of the stimulus signal, the intensity of the twosegment phenomenon is closely related to the amplitude and width of the stimulus signal.

The amplitude of the identical pulse signal is the value of the extra voltage applied on the device or the

electric field that forces the particle migration inside the device. According to the Mott theory in the second part of this review, the applied electric field is the main influence factor of the process of particle drift [104, 110], which is enough to affect the formation rate of CFs at the beginning of a complete CF formation. A simple change in this eigenvalue of the identical pulse signal (from one constant to another) was verified to change the state distribution of the memristor device. This change manifests itself as an increase in  $G_{max}$  and a steeper conductivity modulation curve [22, 104] (Figure 7B). In detail, the blue curve with the lowest pulse amplitude in this graph shows the lowest NL and  $G_{\text{max}}$ , and the red curve with highest pulse amplitude in this graph shows the highest NL and  $G_{\max}$ .

For features of the red, the reason is that the increased electric field, caused by the increase in the pulse amplitude, promotes particle drift, so as to increase the number of Vos forming the CFs in the initial state. The conductance value increases because of that, which results in an increase in NL. In short, it is useless to optimize the NL by changing the amplitude of the identical pulse signal. The timing characteristics of the stimulus signal include the duration (called the pulse width  $(t_{width})$  in the pulse signal) and time interval  $(t_{interval})$  of the signal. Both have an impact on the conductance modulation process.

In biology, the frequency of the external stimuli is the key to the human brain's ability to produce memory. According to the multiple memory model proposed by Atkinson and Shiffrin, the biological brain can produce short-term memory (STM) and long-term memory (LTM) as the frequency of the external stimuli to which the bio-synapses are subjected increases [132] (Figure 7C). In experiments and simulations based on memristor devices, conclusions about similar features have also been obtained [32, 133]. Such a feature explains the biological basis for the characteristic that the memristor device exhibits a gradual increase in conductance with continuous external stimulation and provided evidence of a prediction that the frequency of stimulation signals affected the conductance distribution. Figure 7D shows the distribution of the conductance of the memristor device when pulse signals with different  $t_{interval}$ s are applied as external stimuli. Stimulated by a pulse signal with a longer  $t_{\text{interval}}$ , the device has a denser conductance distribution than the one with shorter  $t_{\text{interval}}$  over the same range of conductance values. From the analysis of the intuitive characteristic of the device such as current-voltage (I-V) characteristics, when the  $t_{\text{interval}}$  of the stimulus signal is long enough, the state of the device caused by the previous stimulus signal has enough time to decay back to the state before the stimulus. Conversely, when the stimulus signal  $t_{inter}$ <sub>val</sub> is sufficiently short, the state of the device caused by the previous stimulus signal cannot be returned to its pre-stimulus state even if decay has occurred, when the next stimulus signal arrives. Such a process results in the device being able to maintain a continuous state change.

Analyzing from the perspective of the PDEs model, in conjunction with the calcium ion (Ca<sup>2+</sup>) model in biology [134, 135] related to synaptic weights update, a secondorder memristor model was established by Kim et al. [98]. In this model, the temperature in the device bulk (T), which affected the first-order internal state variable w, while being affected by w, is considered as a second-order internal state variable. In this model, T is no longer considered as a non-critical constant, but rather Joule heating is considered as a major contributor to particle diffusion in the device bulk in the RS process. In fact, Stefano et al. [95] obtained the result that T would be different in the process of the CFs forming by simulation in 2012. Goodwill et al. [136] carried out simulations and experiments to indicate that the  $V_0$  flow would be affected by T. Both the fitting results between the calculation data with experimental data and the similarity between the device and bio-synapses do have better results in this model. The device has spontaneous heat dissipation in the device bulk, resulting from heat exchange between the device bulk and the outside or heat release from the electrodes. When the  $t_{\text{interval}}$ is long, Joule heating due to the complete process of the CFs cannot form heat accumulation in the device bulk. As a result, the heat generated within the device bulk cannot promote the particle diffusion process inside. Therefore, the complete process of the CFs is mainly driven by ion drift, and the RS process of the device will tend to be flat. On the contrary, a great number of heat accumulation leads to the enhancement of the particle diffusion process, so that the CFs in the device quickly enters the complete state. In addition, for  $t_{width}$ , a pulse signal of appropriate length allows the device to be controlled with a continuous RS process. When  $t_{\text{width}}$  is too long, a long time external voltage is loaded on the device, and as a result, the RS process of the device tends to be digitized and uncontrollable.

#### 3.2 Abnormal pulse

One of the important means to study the response characteristics and performance optimization of the memristor is to not change the material of the RS layer and the structural composition of the memristor. Changing the characteristic parameters of the external stimulus signal, such as amplitude, width, signal time interval, and so on, is the main research method. In investigating the NL of the conductance modulation of the device, for this nonideal feature, the researchers found that the response of the memristor to the programming pulse tends to be intelligent, which means the NL can be optimized by applying a smarter programming pulse. Jeong et al. [104, 137], Wang et al. [34, 85], and Park et al. [9, 138] are researchers who have done research in this area. After reading the relevant articles in this research direction, we divided the NL optimization based on external stimuli into two categories, namely, the combined pulse and the feedback pulse, mainly according to the shape of the stimulation pulse, and we summarized them in the form of a map in Figure 8.

The combined pulse breaks the characteristic of a single pulse in a single cycle, and the small-amplitude

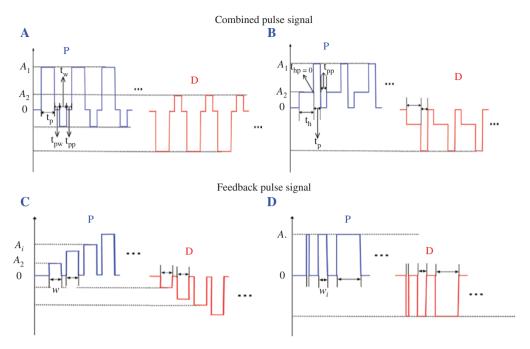


Figure 8: Abnormal pulse signal. (A) Combined pulse signal with the weak anti-pulse. (B) Combined pulse signal with the heating element. (C) Amplitude feedback pulse signal. (D) Width feedback pulse signal.

pulse, called the weak pulse here, is attached with the programming pulse into one cycle as the extra stimulus signal. Figure 8A and B shows this kind of stimulating signal, and the weak pulse of different polarities has a different influence on the weight update of the memristor. When a weak signal is a polar opposite to the programming pulse, called the weak anti-pulse, the effect is to offset the  $\Delta G$  caused by the programming pulse in the previous input cycle. On the contrary, when the weak signal is of the same polarity as the programming pulse, called the heating element, the weak signal is conducive to enhancing the particle diffusion in the device, thus, increasing the  $G_{max}$ . As shown in Figure 8C and D, the feedback pulse uses feedback to process the amplitude and width of the stimulus signal in increments. Each feedback adjusts the next programming pulse according to the previous weight update results to obtain a conductance curve with the lowest NL value. The detail about these two kinds of programming pulse will be explained in sections 3.2.1 and 3.2.2. In schemes of stimulus signal, it is very important to note that the number of stimulus signal has no effect on the characteristic parameters of the memristor response. Enough stimulation cycle make the data more complete, more conducive to data processing and analyzing. According to the data expression of relevant references, the number of signal periods or the time of signal action is used as the abscissa cycle in the study of conductance modulation characteristics. In this review,

the action of the cycle numbers is the same as that of the time as the Abscissa.

#### 3.2.1 Combined pulse signal

#### 3.2.1.1 The weak anti-pulse

Figure 8A shows a typical combined pulse signal, whose feature is the use of the weak pulses with opposite polarity (the weak anti-pulse) [60, 85, 120] to offset the abrupt  $\Delta G$  caused by the training pulse in the first stage, which is the key of this scheme. In this scheme, training pulses are followed by pulses with lower amplitude and duration than the original pulse, whose polarity is opposite to that of the original pulse. It is feasible to achieve the NL optimization and preservation on an on/off ratio by taking the appropriate value of the conductance offset ( $G_{offset}$ ), which is a concept pointed out by Wang et al. [85] in 2016. There is an equation that explains the relationship between realtime conductance  $(G_{(n)})$  and  $G_{\text{offset}}$  (Eq. (7)) [85]. In order to record the conductance value of the memristor after the effect of the previous programming pulse, reading pulses with very small amplitudes are applied after each programming pulse in the study. The number of pulses is used as the time axis to record the conductance value at the corresponding time. By processing the conductance value, and the difference conductance values, means that the  $\Delta Gs$  of each state change are obtained. The  $\Delta G$  is included in Eq. (7), in f(G), and the f(G) means a fit function related to the experimental results.

$$G(n) = G_{\text{initial}} + f(G) + G_{\text{offset}}$$
 (7)

Eq. (7): G(n) is the conductance value after the nth pulse,  $G_{\rm initial}$  is the initial conductance before training, and  $G_{\rm offset}$  is the offset value induced by the weak anti-pulse.

The reason why the pulse signal with the weak antipulse is useful in reducing the value of  $\Delta G$  is that the weak anti-pulse can offset part of the accumulated charges, caused by the previous training pulse, at the interface between the electrodes and the RS layer, which results in the reduction of the electric field. The weakened electric field not only inhibits the process of ion drift but also suppresses the ions that are farther away from the CFs in the interface, and because of that the slope of conductance modulation curve in the first stage eventually becomes slower and slower (Figure 9A). The NL value, as defined in Eq. (1), of the identical programming pulse sequence, is about 0.6~0.81, which is about 0.42~0.54 of the optimized one. This result proves that the combined pulse signal with the weak anti-pulse has a practical significance for the optimization of NL. As shown in Figure

9B, both  $G_{\rm max}$  and NL are all infected by the value of  $G_{\rm offset}$ .  $G_{\rm offset}$  has a value of 0, which means that the identical pulse is applied to the memristor device as the stimulus signal.  $G_{\rm offset}$  has a maximum value of 27 nS, because the maximum value of  $\Delta G$  is 27nS when applied to the identical pulse. The conclusion drawn from Figure 9C is that the greater the value of  $G_{\rm offset}$  is, the smaller is the NL of the device.

The conclusion that should be drawn from the mentioned results is that in order to get the overall improvement of the properties of a memristor when optimizing on NL, it is very important to select the weak anti-pulse with appropriate parameters. In addition to the value of  $G_{\text{offcet}}$ , the time interval between the weak anti-pulse and the programming pulse  $(t_{pw})$ , the time interval between two pulse pairs  $(t_{pp})$  and the duration of the weak antipulse  $(t_{w})$  should all be considered as influencing factors in the optimization process. Considering that the energy consumption and the space of the system are pointed as the focus object when the researchers implement the neuromorphic calculation, the NL optimization of the memristor device should be as close as possible to this point. The implementation of this signal is not complicated, which only needs to use a two-pulse signal generator [85].

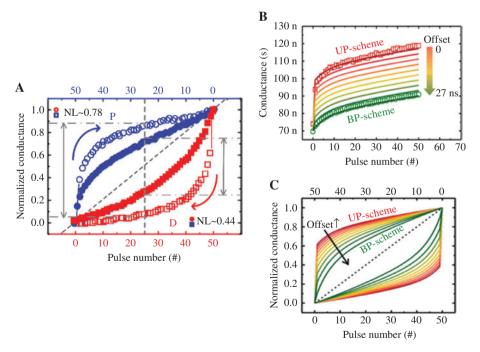


Figure 9: Characteristics of the memristor response to the weak anti-pulse based on the 3D two-layer  $Ta/TaO_x/TiO_2/Ti$  memristor device. (A) Measured conductance modulation curves obtained by applying different pulse signal. Hollow point: response to the identical pulse. Solid point: response to the weak anti-pulse. Adapted with permission from [139]. Copyright 2016 Springer. (B) Simulated conductance modulation curves in different  $G_{\text{offset}}$ . (C) Relationship between  $G_{\text{offset}}$  and NL. Reprinted with permission from Ref. [139]. Copyright 2016 Springer.

#### 3.2.1.2 The heating element pulse

Figure 8B shows another kind of combined pulse signal, whose feature is the use of the weak pulses with the same polarity (the heating element) to enhance the particle diffusion process by rising the local temperature in the device bulk at the beginning of extra stimulation. Specifically, the pulse signal in this scheme consists of a heating element with lower amplitude and a programming element with a higher amplitude. The heating element will not lead to the RS process [85], and the RS behavior happens until the programming element arrives. Because of the considerations of temperature in the memristor device bulk in the second-order memristor model, the separation of stimulation signals for the two elements is considered as a kind of optimized scheme in NL.

The reason why this scheme works is that, in the case of applying an identical pulse on the device, the ions in the area near the CFs and farther away from the CFs are already exhausted, and the ions in the area far away from the CFs have difficulty in migrating to the area where the CFs are located, which limits further expansion of the CFs. However, in the case of applying a state-separated pulse, they promote the ions in the area far away from the CFs to migrate to the area where the CFs are located because of the enhanced diffusion process, which can further expand the CFs. The enhanced diffusion process is caused by a heating element, which leads to the local temperature rise. So the value of  $G_{\rm max}$  can be improved, and the NL can be optimized by the scheme here.

In this scheme, the frequency characteristics of the pulse pair signal are important. Among them, the time interval between the heating element and the programming element  $(t_{\rm hn})$ , the time interval between two pulse

pairs  $(t_{nn})$ , and the width of heating element  $(t_h)$  are all considered as influencing factors in the optimized results. Only when  $t_{\rm hp}$  is small enough does the heating element have a connection to the programming element, driving the memristor to a better state with higher conductance. Therefore, in Figure 8B, the  $t_{\rm hn}$  is shown as zero. Figure 10A demonstrates that as the  $t_{nn}$  decreases, the range of  $\Delta G$  becomes larger, and the slope difference between the two-stage tends to be smaller. The  $t_h$  must be longer than or equal to the time constant [98, 104] of the device, which means the duration or time required for the device to reach a thermally stable state. The application of a heating element with the duration longer than the time constant would not lead to a further increase in local temperature and measurable differences in the RS behavior. However, the duration being shorter than the time constant would lead to the result that the heating element cannot complete the task of reducing NL to the maximum extent. Yeon Jeong et al. [104] applied the pulse signal involved in this section for the NL optimization results. The conductance modulation curve of the memristor device, stimulated by the pulse signal with heating element, has a higher value of  $G_{max}$  and a smaller difference in slope than the one with identical pulse (Figure 10B).

#### 3.2.2 The feedback pulse signal

Another type of abnormal pulse signal is the one that is practically suitable, called the feedback pulse signal [15, 37, 48, 140], because it requires a complicated signal generation circuit as a peripheral circuit of the memristor

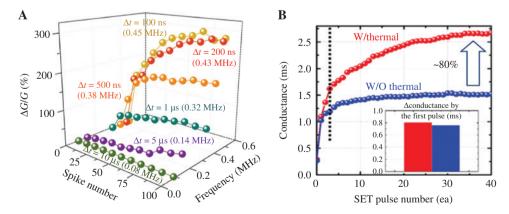


Figure 10: The response of the memristor to the pulse signal with different frequency characteristics. (A) Memristor conductance change as a function of the number and the frequency of the pulse. Adapted with permission from Ref. [98]. Copyright 2015 Nano letters. (B) Measured conductance modulation curves obtained by applying different pulse signals. Blue, the identical pulse; red, the pulse signal with the heating element. Inset shows the comparison of the difference between adjacent conductance when the device is programmed with the two kinds of programming schemes. Reprinted with permission from Ref. [104]. Copyright 2015 Applied Physics Letters.

device. However, it is worth noting that, in theory, it has the best optimization effect on the NL optimization problems (Figure 11). Neeraj et al. [131] showed in their article that the PCMO-based two-terminal memristor in their experiment had an NL of approximately 0 under pulsed feedback stimuli. Similar effects can be achieved with similar strategies based on the TaO, [41] memristor. Conductance of the memristor device obtained by applying an identical pulse is not predictable, as related to current conductance state. Therefore, the NL can be optimized by setting the parameters of the next programming pulse by judging the current response. The scheme in this section is called the programming scheme based on pulse feedback, which can be divided into the amplitude feedback pulse and the width feedback pulse. The purpose is to get a consistent  $\Delta G$  by applying a training pulse sequence with different parameters in each pulse cycle, so that the slope of the conductance modulation curve tends to be consistent. A pulse with shorter duration (or lower amplitude) corresponds to a larger  $\Delta G$  in the original scheme, and the pulse with a longer duration (or higher amplitude) corresponds to a smaller  $\Delta G$ . Both the two strategies can achieve optimization on NL.

For its shortage on complex peripheral circuits, at least one additional computing unit and a special signal generator are needed to comply with the input. A system with a synaptic array cannot achieve parallel weight updates because of feedback. Therefore, the space occupied, the circuit delay, and the energy consumption of the system will be significantly increased, which is not conducive to achieve a large-scale system. Only in theory, have these kinds of schemes any research value.

## 4 Memristor with the multi-RS layer

The original memristor had a simple sandwich structure that contained only one dielectric layer and only one kind of element except the element oxygen or the element nitrogen. Although the traditional structure is easy to implement in the process, it cannot achieve the desired performance for the current pursuit of device optimization. With the development of research, researchers tend to make a dielectric layer diversification by doping or making a multi-layer. The same approach is used in the NL optimization direction, and the desired effect can also be achieved. Xiao et al. [114] had different experimental results by doping in the RS layer. Matveyev et al. [10, 90] got it by making a multi RS layer. Gaba et al. [123] got it by making a multi RS layer, too. With the deepening of research, it has been gradually found that two or three layers of different kinds of dielectric layers have various degrees of optimization effects on the performance of the device. The use of materials with different oxygen contents as a component of the multi-RS layer has proven to be effective in confining the location where the CFs break down to smaller areas in the device bulk so that the performance of the device especially the stability is improved. A similar approach can be achieved on the issue of NL optimization. The difference is that in the NL optimization problem, from a material point of view, researchers need to consider the particle migration state inside, including drift speed and thermal diffusion. The combination of materials have different particle migration effects as the multi-RS layer of the device is verified to achieve the goal of controlling the device conductance distribution [102, 141, 142].

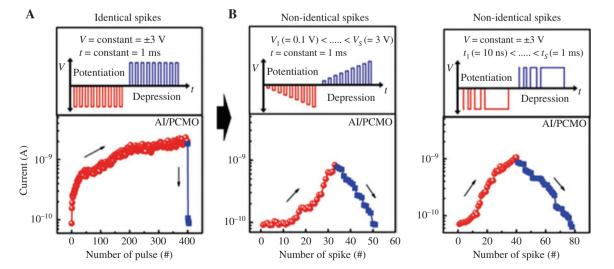


Figure 11: Characteristics of the memristor response to the feedback pulse signal based on the TE/Al/PCMO/BE memristor device. Reprinted with permission from Ref. [139]. Copyright 2016 Springer. (A) Identical pulse. (B) Feedback pulse.

In detail, from Eqs. (2) and (3) derived from the Mott theory, particle migration is largely affected by the environment where the particles are located [143, 144]. Therefore, it is feasible to reduce the number of particles that participate at the beginning of conductance modulation by limiting the rate of particle migration, to achieve the purpose of slowing down the process of forming complete CFs. A viable program is to insert one or more layers with materials that can suppress particles migrating between the basic RS layer and the top electrode (Figure 12). Layers inserted are called the migration limit layer (MLL). Zongwei et al. [36] named their insert layer as an ion diffusion-limiting layer (DLL).

The PDE model shows that in the set process, under the stimulation of a directed external voltage, the  $j_{drift}$  and  $j_{
m diff}$  are in the same direction at the beginning, and the diffusion process promotes more particles to participate in the process of CF completeness. With the extension of stimulation time, due to the gradient distribution of the carrier concentration, the direction of  $j_{\text{diff}}$  is perpendicular to the direction of  $j_{drift}$ , as shown in Figure 5, resulting in the horizontal expansion of the CFs. The main influence of the drift process is the applied voltage stimulus. Therefore, from a material point of view, by controlling the diffusion process, the number of particles that previously participated in the RS process at the beginning can be limited. The purpose of doing so is to depress the high slope of the conductance modulation curve in the first stage, prompting NL optimization.

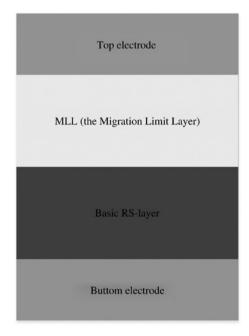


Figure 12: Model of the memristor with the MLL.

From the equation  $D = D_0 \exp(-E_c/kT)$  for the diffusion coefficient, the diffusion coefficient of oxygen (D) can be obtained. The materials of the MLL tend to choose the one with  $D_{\nu}$  less than that of the basic RS layer to achieve the NL optimization. In addition to the temperature of the device bulk, the two main influencing factors for D<sub>v</sub> are "a" and " $E_a$ ". The former is usually assumed in the calculation, the hypothesis is set at 0.05 nm ~0.5 nm [56], and the final simulated value depending on the fitting results of the calculation data and experiment data. "a" appears as a hypothetical value in the calculation. In the PDEs model ignoring the effect of the electrode heat release on the temperature in the device bulk, Kim et al. [56] drew a set of conclusions based on a series of reasonable assumptions, excluding the effect of electrode heat release on the temperature in the device. The calculation curves in the conclusion show that the larger the value of a, the more the device tends to be digitized, which means the larger the NL degree. This trend is unfavorable to the application in the field of the neuromorphic system. Table 3 lists the hypothetical values used in the calculation of several materials for reference. The latter is the activation energy for the hopping process, and the greater its value, the harder it is for the particles in the material to transition. Similarly, Table 3 lists the values of  $E_a$  for several materials. SiO<sub>2</sub> is a typical semiconductor material with an  $E_a$  value in the range of 0.92 eV-1.71 eV and an average level higher than the other oxide semiconductors in Table 3. The  $D_{\nu}$  of SiO<sub>2</sub> is about  $10^{-24}$ – $10^{-20}$  cm<sup>2</sup>/s [55, 72] at room temperature, which is one or more orders of magnitude lower than that of other binary metal oxides. For example, it is lower by one to six orders of magnitude compared to TaO, [140, 149]. Zongwei et al. [36] inserted SiO<sub>2</sub> as the MLL on the basic layer of TaO, in a memristor device. After comparing the memristor

Table 3: Summarization of diffusion constants of some dielectric layers corresponding to an oxygen.

Assumption value	Material	Reference	
a (nm)			
0.1	TaO <sub>x</sub>	[56]	
0.1	HfO <sub>x</sub>	[94]	
0.15	WO <sub>x</sub>	[145]	
0.3	$Al_2O_3$	[146]	
_			
Ea (eV)			
0.4	$WO_x$	[145]	
0.85	TaO <sub>x</sub>	[69]	
0.9	Al <sub>2</sub> O <sub>3</sub>	[146]	
1	HfO <sub>x</sub>	[147, 148]	
0.92~1.71	SiO <sub>2</sub>	[69]	

devices with different thicknesses of  $SiO_2$  (1 nm, 2 nm, 4 nm), they concluded that the NL of the device is obviously optimized when the MLL of  $SiO_2$  is 2 nm (Figure 13).

Finding the right kind of MLL material is the basis of NL optimization. In detail, the MLL with appropriate thickness can weaken the slope of the conductance modulation curve in the first stage, which is good for NL optimization. As shown in Figure 13A, when the thickness of SiO is 1 nm, the NL of the conductance modulation is significantly reduced, and the on/off ratio of the device is about 0.7, which is not too small compared with that of the device with no MLL. However, when the thickness is 4 nm, the  $G_{max}$ is about 25% of the no MLL device, and the on/off ratio is only about 20%. As the thickness of the MLL increases, the length of the area where CF growth is limited increases. This results in an increase in the distance where particles need to move in a limited area. Over-thick MLL inhibits the diffusion process and the horizontal expansion process of the CFs in the memristor device. Therefore, the  $G_{\max}$  of the device is significantly reduced. Although the decrease in the  $G_{max}$  will lead to a reduction in energy consumption of the device [96], there is a significant reduction in the on/ off ratio, which is inconsistent with the purpose of device optimization. Furthermore, the SiO<sub>2</sub> thin film formed by

sputter deposition has a poor microscopic density compared with that formed by evaporation deposition [54]. The poor microscopic density results in a larger ion migration rate to give a more obvious effect on NL optimization.

## 5 Summary of the optimization scheme

The optimization schemes on the conductance modulation of the memristor in this review are mainly divided into two categories: applying a smarter programming pulse and changing the structure of the memristor. These schemes have different NL optimization effects, and there are differences in the ease of implementation. In order to make the paper more directive and intuitive, the advantages and disadvantages of the schemes are classified and summarized in this section. Objects are summarized in addition to the optimization schemes in the review and also those outside the scope of discussion but contributing to the direction of NL optimization. The above schemes are classified from three aspects: NL optimization, feasibility, and novelty degree.

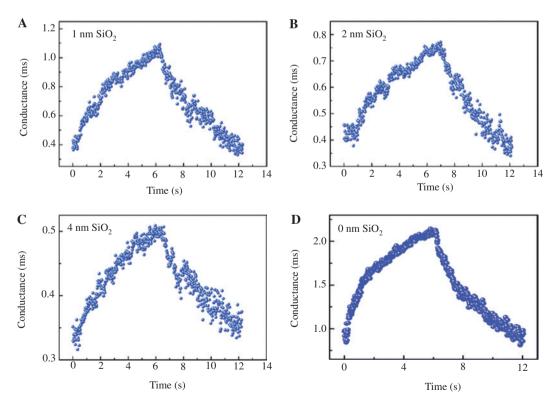


Figure 13: Conductance modulation curves obtained in memristive devices with  $SiO_2$  as the MLL with different thicknesses. Adapted with permission from Ref. [69]. Copyright 2016 Nanoscale. (A) TiN/1 nm-SiO $_2$ /TaO $_x$ /Pt memristor device. (B) TiN/2 nm-SiO $_2$ /TaO $_x$ /Pt memristor device. (C) TiN/4 nm-SiO $_2$ /TaO $_x$ /Pt memristor device, with no DLL.

For an identical pulse scheme, it is also possible to obtain a lower NL by changing the initial conductance, the pulse amplitude, or the pulse width. It is important to note that methods such as increasing the number of pulses have no effects on NL optimization. From a realizable point of view, uplifting the initial conductance can significantly reduce NL while largely reducing the on/off ratio. It is pointed out that optimizing NL by increasing the amplitude of the input pulse is useless, the results of which will be an increase in the maximum  $\Delta G$ , not the NL optimization.

In the four kinds of pulse schemes mentioned above. the combined pulse schemes have obvious advantages over the feedback pulse schemes in terms of feasibility, which are mainly manifested in the stimulus signal generation module. The feedback schemes can get the most suitable stimulus signal by processing the response generated after each cycle and feeding back to the stimulus signal-generating module. Therefore, the complex stimulus signal generation and processing module is needed, and the feasibility is low. However, because of this, the feedback schemes can achieve almost an ideal NL optimization. Because the generating module of the stimulus signal requires extra consumption, the pulse scheme is weaker than the structural scheme in terms of feasibility and energy consumption. From the perspective of novelty, the pulse optimization scheme depends on the optimization of the three PDEs in theory. For example, the firstorder memristor model is optimized to the second-order memristor model, which is dependent on T and w. It is of great significance to the performance optimization and theoretical model of the memristor.

Schemes with a multi-RS layer are immature; they has an advantage in simplifying the weight update process and the peripheral circuits compared to the other schemes, and it is feasible to achieve NL optimization by choosing suitable TE materials. In the aspect of feasibility, this scheme is superior to the pulse optimization schemes. The materials and structures of the RS layer of memristors are the main means of research in this field, which can achieve different optimization effects. Therefore, in these schemes, the novelty is attributed to the pulse optimization schemes.

This review focuses on memristors based on binary metal oxides, but there are also some related studies on NL optimization in the types of memristors outside this range. As shown in Table 2, it is worth noting that organic compound-based memristors, one of the main research directions of memristors, have NLs with excellent value, although their other aspects (like the on/off ratio) do not reach the same level as the metal oxide-based memristors.

With the deepening of research, more and more research on memristors is using polymetallic oxides as materials of the RS layer, to achieve the goal of device optimization. Among them, Nili et al. from RMIT University conducted research on Nb-doping STO-based memristors [150]. In their research, Nb:a-STOx-based memristors show a high degree of uniformity and durability, and a lower NL of the conductance modulation results can be obtained by adjusting the partial bias amplitudes. It is worth noting that this study places the temperature and thermal effects of the device in an important position, which is the current research trend. As the upgrade structure of the two-terminal memristors, the three-terminal device [61, 63, 72–78] can achieve a good balance in NL optimization and other aspects, like energy consumption.

## 6 Application on neuromorphic learning

Synaptic circuits are used as a connection layer between two neuronal layers, which can use the memristor as the basic unit, to be components of a neuromorphic system [12, 151]. A hardware circuit system combines corresponding algorithms, like sparse coding algorithm, to achieve tasks [26, 138, 152-158] like image recognition. In the image recognition system, binary black and white images are made as the training objects. The system can store it after training, which means learning under stimulation from a training pulse.

In such an identification system, learning accuracy [11] is an important parameter to demonstrate the ability of such neuromorphic systems to accept and correctly identify what they learned, and conductance maps of the system can give a direct impression about it. The factors that may affect the learning accuracy include the NL of the weight update, the on/off ratio, and the device variations at the device level. In this section, the improvement of learning accuracy at the system level caused by optimized NL at the device level is analyzed.

Figure 14A shows the simulation results of a recognition system with  $8 \times 8$  synapse cells [85]. The purpose of the system is to identify an  $8 \times 8$  binary alphabetic "B" pattern with 10% error bits in each  $8 \times 8$  training pattern. This indicates the initial state when the training period is 0. The initial weights of the synapses, which means the initial conductance of the synaptic memristors, are randomly distributed, as shown in Figure 14A. When the synaptic elements have an ideal linear weight update, the learning results gradually become obvious with an

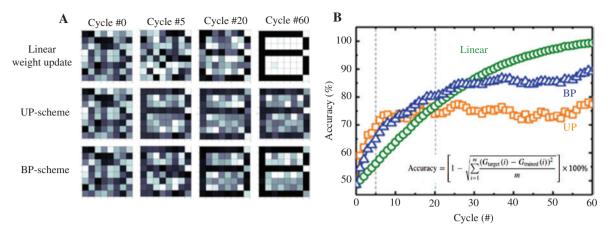


Figure 14: Changes in learning accuracy at system level caused by optimized NL at device level. Adapted with permission from Ref. [139]. Copyright 2016 Springer. (A) Comparison of the simulated training weight map of an 8 × 8 binary alphabetic B pattern when the device is programmed with three weight update schemes. The first column, linear weight update scheme; the second column, scheme based on identical programming pulse; the third column, scheme based on the weak programming pulse with opposite polarity. (B) Comparison of the simulated training accuracy, defined by equation inset, when the device is programmed with three weight update schemes. Inset shows the difference in NL between two kinds of programming schemes (identical pulse, the weak pulse with opposite polarity).

increase in the training cycles. After 60 training cycles, the learning process is completed with a learning accuracy of 100%, which has no error bit.

When the synaptic elements are in the memristor device with a vertical double-layer structure based on tantalum oxide [159], the learning results are shown as fast close to saturation. However, the learning accuracy is only about 78% at the end of the stimulation, in which there are many error bits, as shown in Figure 14B. The reason for the higher learning outcome after the fifth training cycle, as shown in the second column in Figure 14A, can be attributed to the abrupt RS behavior of the synaptic device initially. As shown in Section 3, the scheme with the weak anti-pulse can reduce the NL level of the synaptic device by one level. The third column in Figure 14A

shows the learning results based on this scheme. This shows a gradual situation, and the number of error bits is gradually reduced.

Compared with the learning accuracy based on the memristor synaptic devices with a different NL, it can be concluded that the learning accuracy of the system is affected by the NL of the device, as shown in Figure 14B.

However, optimization on NL would also change other performances [11] like the on/off ratio. Therefore, the above results can only indicate that the NL has an impact on the learning accuracy, but cannot explain which factor causes it specifically.

Figure 15A shows a map of the learning accuracy in a neuromorphic system [11] based on the NL-level table as shown in the inset of the graph. In the case of a perfectly

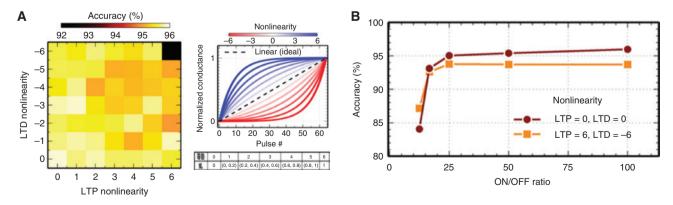


Figure 15: Chain effects caused by optimization on NL. (A) Comparison of the learning accuracy with different LTP and LTD non-linearities. Right, different non-linearity of the LTP and LTD fit from 0 to 6 and the level table about NL. Adapted with permission from Ref. [139]. Copyright 2016 Springer. (B) Learning accuracy with different on/off ratios. Reprinted with permission from Ref. [139]. Copyright 2016 Springer.

symmetrical distribution of the LTP and LTD, when the NL level increases from 0 to 4, the learning accuracy of the system decreases gradually. When the NL level continues to rise to level 5, there is a slight increase in the learning accuracy. When it rises to level 6, there is a significant reduction in the learning accuracy. Figure 15B shows that in this system, when the on/off ratio of the device is reduced to less than 25, the learning accuracy of the system is significantly reduced. However, there is no obvious change. Although these results are based on a certain algorithm, we can give the following inspiration: (1) The on/off ratio of device has a threshold that determines the learning accuracy of the system. (2) There is a key point where NL is the main factor causing the learning accuracy optimization or deterioration.

In summary, the NL of the weight update has direct and indirect effects on the learning accuracy of a neuromorphic system. The indirect effects are caused by the properties associated with NL. Optimized NL will inevitably change the other properties of the device, which will result in the improvement in the system learning accuracy.

### 7 Summary and prospect

Although there is no uniform standard for the RS mechanism yet, its scope has been gradually narrowing down along with more and more research about memristors turning up in recent years, and the non-ideal features of the memristor are more unignorable in the exploration of the RS mechanism. Especially, a lower NL of a conductance modulation is found to be helpful not only in establishing a mathematical model of the memristor with a higher fitting degree [67, 144, 159] but also in helping to improve the recognition accuracy of the neuromorphic system. The ultimate goal of doing optimization at the device level is to achieve systems with excellent performance. Based on this purpose, optimization on a device needs to find balance between all the associated properties.

Using the Mott theory and the three PDE models as a theoretical support for the RS process of the memristor device, we analyzed the reason for the NL based on the particle migration theory. Based on these theories, the formation process of the CFs inside the memristor has obvious stage phenomena. We do work summarizing the NL optimization scheme into two categories, applying smarter programming pulse and changing structure of the memristor, through the related experimental research, and analyzed their advantages.

The programming pulse signal has a significant influence on the CF formation process and internal temperature change and particle migration inside the memristor. In the aspect of NL optimization, the intensity parameters and timing parameters of a pulse signal have a certain influence on  $\Delta G$  and  $G_{max}$ . However, when the identical signals are as a stimulus, these parameters have no real impact on NL optimization. Therefore, the abnormal signals become more and more common in the related research. It is important to find a suitable extra pulse for the scheme for using the combined pulse signal. The design of this kind of signal is based on the three PDEs, and its experimental results can prove the correctness of the three PDEs while optimizing its solution process to obtain the simulation result with a higher fitting degree. The feedback pulse signal is another kind of optimization scheme, and it is achievable to obtain the optimal degree of NL using this programming pulse signal in the simulation. However, in the actual research, to realize this simulation physically, it is necessary to solve the problem of simplification of the complex degree of the signal-generation module, or the scheme has no practical application or value at the system level. NL optimization from the perspective of changing the component structure of the memristor has the same substantive effect. The main basis of this kind of scheme is to restrict the distance and speed of the particles moving inside the memristor by doping or MLL. One of the things that needs special attention in both scenarios is that changes in NL optimization may cause changes in its associated object, such as the on/ off ratio or circuit complexity.

The final beneficiary for optimization at the device level should be the system. It is important to note that NL is an important factor that cannot be ignored in the field of application of neuromorphic systems, and we call it the relationship between the learning accuracy of the system, based on the memristor synaptic device, and the NL of the memristor. It has both a direct relationship and an indirect relationship. In the case of different systems and algorithms, NL has a different proportion of influence on learning accuracy, and its associated objects to the system will be different. It can be hypothesized that there are thresholds in NL optimization. When properties associated with the NL are lower than a threshold, NL optimization may be meaningless. At the system level, the stability, large-scale miniaturization, and low power consumption are the main research directions now. Therefore, optimization on a device must consider them. As regards NL optimization, doing optimization in the structure of the memristor is better considering space and energy. However, in both, the two categories of schemes in NL optimization, still more work that is valuable needs to be done in the future. Other non-ideal properties of the memristor also have limitations on its development and the neuromorphic system. Research on optimization needs to be continued in the future.

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#### **Bionotes**



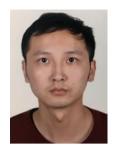
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