

Review

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Design of reversible logic circuits using quantum dot cellular automata-based system

DOI 10.1515/ntrev-2015-0033

Received May 29, 2015; accepted July 31, 2015; previously published online September 29, 2015

Abstract: Shrinking transistor sizes and power dissipation are the major barriers in the development of future computational circuits. At least when the transistor size approaches the atomic scale, duplication of transistor density according to Moore's law will not be possible. Physical limits, like quantum effects and nondeterministic behavior of small currents, and technological limits, such as high power consumption and design complexity, may hold back the future program of microelectronic conventional circuit scaling. Hence, an alternative technology is required for future design. Quantum dot-cellular automata (QCA) is a transistor-less, very promising nanotechnology that can be used to build nanocircuits. The conventional computer is an irreversible one; i.e. once a logic block generates the output bits, the input bits are lost. A possible solution is reversible computing, where no bit is lost during computation. Hence, logically reversible circuit can consume less energy than any conventional circuit. In this paper, a brief review on evolution of the QCA in reversible computing is discussed. Various reversible gates that are designed using QCA technology as well as the modification of those designs that are made in latter works are highlighted.

Keywords: nanotechnology; quantum dot cellular automata; reversible logic circuit.

1 Introduction

In 1961, Rolf Landauer of IBM defined a revolutionary principle that when the output of any logical circuit does not uniquely define its input, then the device is said to be logically irreversible and it will dissipate energy [1]. Logical irreversibility means that any outputs from a logic gate can be obtained from more than one set of inputs. For example, the logic gate AND $(A, B)=Y$ that maps two input bits, A and B , into a single bit, Y , is logically irreversible because an output $Y=0$ (false) could be accounted for by any of the three input pairs $(A=0, B=0)$, $(A=0, B=1)$, and $(A=1, B=0)$. Hence, for this particular output, the input is ambiguous and the operation is said to be logically irreversible. According to the second law of thermodynamic consequences, whenever a logically irreversible operation is performed, energy must be dissipated, in the amount of $k_B T \ln 2$ J per bit erased [1], where k_B is the Boltzmann constant and $T=300$ K. This value is equivalent to $\sim 2.9 \times 10^{-21}$ J at room temperature. This was also experimentally proven by Bèrut et al. [2]. When bit is destroyed inside the circuit, entropy of the physical system increases according to the second law of thermodynamics. Thus, heat dissipation in a circuit can be expressed by Shannon entropy (H) as $-\sum p_i \ln p_i$, where p_i is the probability of state during computation. If ΔH measures the logical entropy changes in bits, then minimum heat dissipated is $\Delta E = k_B T \ln 2 \cdot (\Delta H)$. If total change of entropy of system and the surrounding is >0 , then a physical system cannot run in reverse. Thus, the system is called thermodynamically irreversible. The energy E bit required for a binary transition is given by the Shannon-Von Neumann-Landauer (SNL) expression in [1, 2] as follows:

$$E \text{ bit} \geq E_{\text{SNL}} = k_B T \ln 2 = 0.017 \text{ eV.} \quad (1)$$

This amount is small but not negligible for a large circuit. Also, at low temperatures ($T \rightarrow 0$ K), this will be very low. Also, from the Heisenberg uncertainty relation, the size of the device should be ~ 1.5 nm at room temperature for low loss [3]. Hence, a nanoscale circuit is required for lossless computing in the future. The solution for

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this energy loss can be obtained by introducing reversible computing. In order to eliminate the problem of bit loss, reversible computing came into practice. Bennett first proposed the principle of logical reversibility. He showed that, asymptotically, zero-power dissipation in logic circuit is possible only if the circuits are composed of reversible gates [4]. There are two types of reversible elements: one without memory, which is usually called a reversible logic gate, and the other with memory, which is called rotary element [5]. In this article, reversible logic elements are discussed. According to the theory of reversibility, any reversible logic gate will follow the following principles:

1. For n bits of inputs, there should be equal n bits of output.
2. The input combination will be reflected at the output but not necessarily in the same order.
3. Fan-out is not possible in reversible systems.

Thus, reversible gates do not erase any information, and consequently, a computation based on reversible logic can be run forward to obtain an answer as well as the answer copied, and then the whole computation is undone to recover almost all the energy expended. A reversible gate has an inverse, that is, a gate that “undoes” the logic function [6]. A logic gate is said to be self-invertible if the gate is equal to its own inverse. For example, a gate G is self-invertible if, for every input x , $G(G(x))=x$ [6]. The unused outputs are used to maintain the reversibility of the circuits and are known as the garbage outputs. However, the inputs that are regenerated at the outputs are not considered as the garbage [7]. The constant inputs in the reversible circuits are called the ancilla. Numerous reversible logic gates have been proposed in following years, out of which some of the notable ones are Fredkin gate and Toffoli gate proposed by Fredkin and Toffoli [7], Feynman gate (FyG) [8], TSG gate [9].

Boolean logic gates are arguably the most important elements of modern computers and switching networks. At the same time, numerous contributors to electronic Boolean logic gates have revolutionized the world by keeping Moore’s law alive. However, it is obvious that such an exponential growth of transistor density on some square millimeters must reach its limits in the future – at least when the miniaturization reaches a level where a single transistor size approaches the atomic scale. Thus, some researchers think that in 2020 to 2025, duplication of transistor density will not be possible any longer. Computers today are based on electronics, but ohmic loss (I^2R) happens when electron moves through wire.

Increase in power consumption is becoming a limiting factor in high-performance digital circuit and systems. In electronics, Ohmic loss cannot be avoided. Quantum dot-cellular automata (QCA) was first proposed by Lent et al. in 1993 in their paper [10, 11]. QCA is a transistor-less technology, and beyond CMOS technology, it will play a vital role in future supercomputing [12, 13]. It is based on the principle of quantum confinement. When a low-bandgap material is confined in three dimensions (3D confinement) by another high-bandgap material, then quantum dot (QD) is formed. QD is a 0D structure, where carries are restricted to a specific set of completely quantized energy states. A QCA cell consists of four QDs, out of which two dots are injected with extra electrons. Depending upon the position of the electrons, the QCA cell gains its polarization. The basic advantages of QCA are the following:

1. It is a transistor-less technology; as a result, it does not face short channel effects.
2. QCA is a charge confined protocol, so it does not have the disadvantage of charge dissipation.
3. QCA circuit operates at a speed of terahertz frequency range.
4. QCAs have high packing density.

This paper is organized as follows, Section 2 will provide a brief overview of QCA cell structure, majority voters (MVs), and clocking. In Section 3, we will focus on different approaches made to design many reversible logic gates. Comparative analysis of all those designs is given in Section 4. Finally, a conclusion of the review is drawn in Section 5, followed by references.

2 Background of QCA

Lent et al. [10, 11] were the first to propose the concept of QCA. QCA is a transistor-less technology. It is based on the concept of charge quantization. QDs are produced by forming semiconductor heterostructure. A QCA cell will consist of four such QDs. Electrons are injected in the QDs, which occupy the corner-most dots of the cell. Depending upon the position of the cell, the polarization of a QCA cell can be determined with three different cell-polarization states, as shown in Figure 1A, viz. $P=0$ (null state), $P=-1$ (binary 0 state), and $P=+1$ (binary 1 state), respectively.

The polarization of electrons can be described with respect to quantum mechanics. The polarization P is defined as follows:

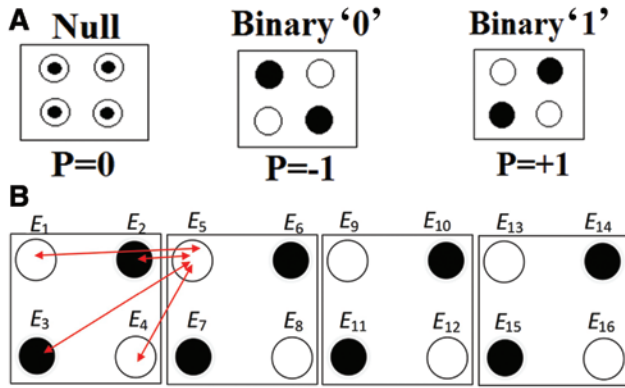


Figure 1: Basic QCA cells. (A) Different QCA cell polarization, (B) data flow in QCA wire.

$$P = \frac{(\sigma_1 + \sigma_3) - (\sigma_2 + \sigma_4)}{(\sigma_1 + \sigma_2 + \sigma_3 + \sigma_4)}. \quad (2)$$

Here, σ_i is the expected value of number operator of site i . For the ground state Eigen functions:

$$\sigma_i = \langle \psi_0 | \hat{n}_i | \psi_0 \rangle, \quad (3)$$

where $|\psi_0\rangle$ represents the ground state. According to polarization P , the electrons are positioned with applied strong stimulation such as heat, voltage, or photons. This can change the electron polarization of the cell due to “kink” the energy. From Coulomb’s law, it is known that the potential energy ($E_{i,j}$) between two charges q_i and q_j separated by distance r_{ij} is given by Eq. (4).

$$E_{i,j} = \frac{1}{4\pi\epsilon_0} \frac{q_i q_j}{r_{ij}} = \frac{k q_i q_j}{r_{ij}} \quad (4)$$

ϵ_0 = permittivity of free space

q_i and q_j = electrical charges of i and j , respectively

$|r_i - r_j| = r_{ij}$ = distance between two electrons

$$k = \frac{1}{4\pi\epsilon_0} = \text{Coulomb constant} \approx 9 \times 10^9$$

Considering the values of k , q_i , and q_j , $k q_i q_j = 9 \times 10^9 \times (1.6)^2 \times 10^{-38} = 23.04 \times 10^{-29} = A$ is obtained [14–16]. The energy represented by Eq. (4) is minimum when two neighboring cells have same polarization and is maximum when they are in opposite polarization. The difference between this maximum and minimum energy is called kink energy, i.e. $E^{\text{kink}} = (E_{i,j})|_{P_i \neq P_j} - (E_{i,j})|_{P_i = P_j}$. $E_{i,j}$ can be calculated using Eq. (4) and can show how data are transferred through the QCA wire, which is QCA cells placed side by side. Here, data or the cell polarization is

transferred through the wire without having any charge transfer. A cell wire is composed of a finite number of cells (say N), all lined up forming a linear array. At the initial condition, i.e. when the system is in ground state, all the cells have the same polarization. Suppose, then, the cell in one extremity of the wire is externally forced to change its polarization, and suddenly a kink in polarizations appears between the first and the second cells of the array. This kink must then propagate through the array until it reaches the other extremity. Figure 1B shows a simple QCA wire having three QCA cells. Here, each dot of QCA cells is numbered from E_1 to E_{16} . Navi et al. [17, 18] have proposed a physical proof of the functionality of QCA devices. They calculated the potential energy of electrons in each dot in a cell with respect to the potential energy of the electron in the previous cell [17, 18]. It was observed that in order to achieve more stability, the electrons in each cell should be placed in such a manner so that their potential energy reaches minimum level.

$$\text{Total potential energy} = U_T = \sum_{l=1}^n (E_{i,j})_l.$$

Here, the cell size is considered 18 nm × 18 nm, and there is a 2-nm gap in between two cells. Let the first leftmost cell at polarization be $P=+1$. At first, we can calculate the potential energy existing between electrons E_1 , E_2 , E_3 , and E_4 and E_5 . Based on the calculation, the position of electrons in cell 2 is defined. Let the potential energy between E_1 and E_5 be $(E_{1,5})_1$ and so on. Therefore, the potential energies are calculated as follows:

$$(E_{1,5})_1 = \frac{A}{r_{1,5}} = \frac{23.04 \times 10^{-29}}{20 \times 10^{-09}} \approx 1.15 \times 10^{-20} \text{ J}$$

$$(E_{2,5})_2 = \frac{A}{r_{2,5}} = \frac{23.04 \times 10^{-29}}{2 \times 10^{-09}} \approx 11.52 \times 10^{-20} \text{ J}$$

$$(E_{3,5})_3 = \frac{A}{r_{3,5}} = \frac{23.04 \times 10^{-29}}{\sqrt{(18)^2 + (20)^2} \times 10^{-09}} = \frac{23.04 \times 10^{-29}}{26.90 \times 10^{-09}} \approx 0.856 \times 10^{-20} \text{ J}$$

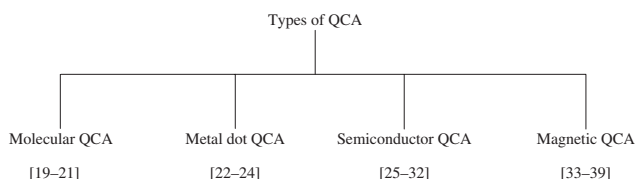
$$(E_{4,5})_4 = \frac{A}{r_{4,5}} = \frac{23.04 \times 10^{-29}}{\sqrt{(18)^2 + (2)^2} \times 10^{-09}} = \frac{23.04 \times 10^{-29}}{18.11 \times 10^{-09}} \approx 1.27 \times 10^{-20} \text{ J}$$

$$\text{Hence, } U_{T1} = \sum_{l=1}^4 (E_{i,j})_l = [(E_{1,5})_1 + (E_{2,5})_2 + (E_{3,5})_3 + (E_{4,5})_4] = 14.796 \times 10^{-19} \text{ J}.$$

In the same way, the potential energy (U_{T2}) of electron E_6 with E_1 , E_2 , E_3 , and E_4 as $(E_{1,6})_1 = 0.57 \times 10^{-20}$ J, $(E_{2,6})_2 = 1.04 \times 10^{-20}$ J, $(E_{3,6})_3 = 0.50 \times 10^{-20}$ J, and $(E_{4,6})_4 = 0.61 \times 10^{-20}$ J, respectively, is calculated. Hence, $U_{T2} = [(E_{1,6})_1 + (E_{2,6})_2 + (E_{3,6})_3 + (E_{4,6})_4] = 2.72 \times 10^{-20}$ J. So, $U_{T2} < U_{T1}$. So, electron E_6 is much more stable than E_1 . Similarly, it is shown that electron E_7 is much more stable than E_8 . So, the second cell will be the polarization $P = +1$; i.e. data are transferred to the second cell. In the same manner by calculation of potential energies for each electron, we can physically determine the polarizations for each cell. In this way, data transfer through QCA wire can happen.

2.1 Types of QCA

There are four types of QCA reported so far. These are as follows:



2.1.1 Molecular QCA

In [19], Lent et al. produced a QD at the redox center of the proposed molecule 1(1,4-diallyl butane radical cation). In [20], Lent et al. proposed another three-dot molecule based on the same principle as in [19]. The molecule proposed in [20] has three allyl groups connected in a “V”-like structure by alkyl bridges. It represents a “QCA half-cell,” which can be in the state 1, 0, or NULL as shown in Figure 2. The isopotential surfaces of three states, i.e. state 1, state 0, and null, are shown in Figure 2. The lump indicates the occupancy of excess positive charge or hole on an allyl group. In [21], an unsymmetrical Ru-Fc complex QCA cell is prepared and synthesized. Further XPS and spectrographic studies are performed to support the experimental observations.

2.1.2 Metal Dot QCA

Several works are proposed in metal dot QCA cell. The metal dot QCA cell fabricated by Orlov et al. [22] is shown in Figure 3. It consists of four metals connected

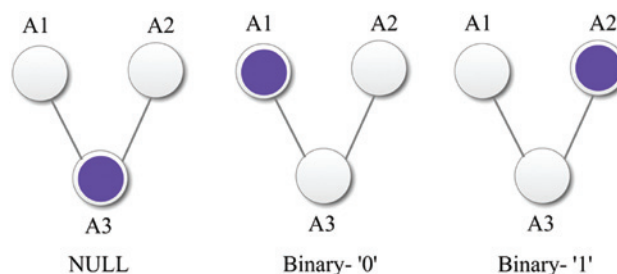


Figure 2: Charge configuration of the molecules proposed in [20]. This molecular structure has 3 allyl groups (shown by three circles by A1, A2 and A3 respectively in ‘V’ shape). Among them, two are neutral and one is positive. In this case positive charge (hole, shown by filled circle) transferred between different dots, creates three states (‘NULL’, ‘Binary-0’ and ‘Binary-1’ respectively).

by Al-AlO_x-Al tunnel junctions. The fabrication is done by electron beam lithography method and shadow evaporation techniques at 15 K temperature. A magnetic field of 1 T is required to generate superconductivity of the metal. Electron transfer between dots creates polarization change. Gate electrodes (on which external voltage is applied) force to tunnel an electron to switch from one dot to the other.

In the metal dot QCA paradigm, the dot is basically a metal island. Tóth and Lent [23] show the quasi-adiabatic switching of a metallic half-cell consisting of three metal islands. Here, the top and bottom islands will correspond for the polarization of the cell, whereas the null state will be associated with the middle island. A leadless QCA double dot cell had been fabricated by Amlani et al. [24]. Here, the metal island is made of aluminum. The area of the tunnel junction fabricated is $60 \times 60 \text{ nm}^2$ and electron temperature is 70 mK. The fabrication here is also done by electron beam lithography.

2.1.3 Semiconductor QCA

A QCA cell can be realized in silicon system [25–27]. In a semiconductor material like GaAs/AlGaAs, four QDs can be fabricated with a high-mobility 2D electron gas (2DEG) below the surface. The idea of patterning electrons confined in 2DEG using metal top gate has been implemented to develop semiconductor QCA system. The 2DEG is formed at the interface of a semiconductor substrate and dielectric layer. The preferable semiconductor materials are silicon-silicon dioxide or III–V heterojunction materials. Electric field is applied through the metal top gate, which depletes the electrons in the 2DEG. Finally, metal gates are etched

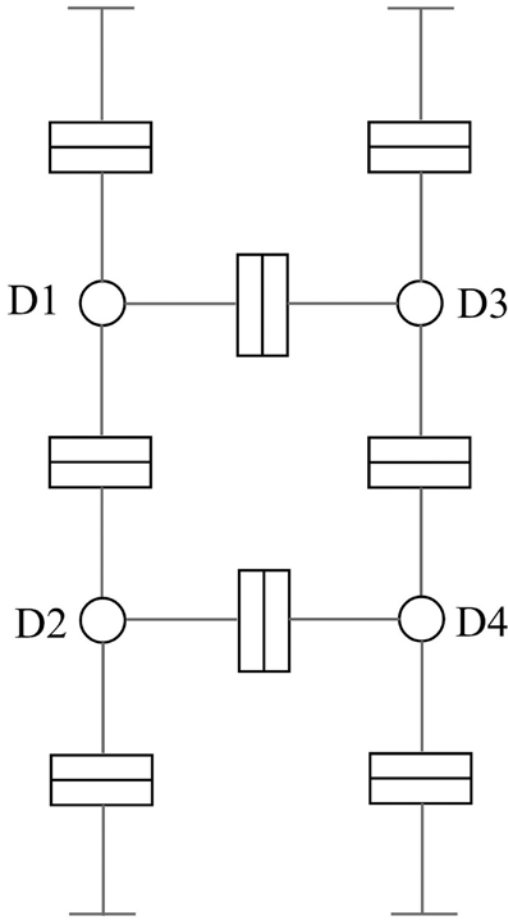


Figure 3: Schematic of metal dot QCA.

away to form QDs at the exposed surfaces. In [28], Lent and Tougaw have proposed the possible fabrication of semiconductor QCA system with this technique. Further, the authors in [28] have modified the structure to develop a sharper QD. This is by using dual metal top gates. The fabricated layout demonstrated by Lent and Tougaw [28] is shown in Figure 4. Here, two top metal gates (G1 and G2) control the occupancy of electrons in p-type Si substrate. A lower metal gate is used to deplete holes near the surface of the metal substrate where QDs are not desired. Using this approach, dots can be made to hold a single electron. This design can be fabricated with scanning tunneling lithography [29, 30].

QDs are formed by 3D confinements of semiconductor materials with different lattice structures [31]. There are two types of semiconductor junctions, viz. homo-junction and hetero-junction. Homo-junctions are formed at the interface of two semiconductors of similar lattice structures, whereas hetero-junctions are formed at the interface of two dissimilar crystalline semiconductors. The thickness of the layer at which the QDs are formed is

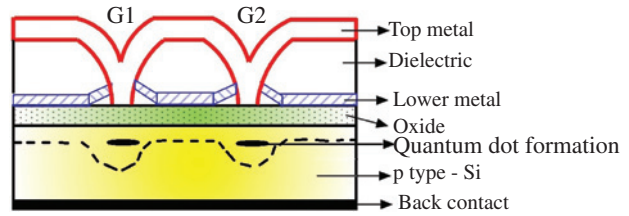


Figure 4: Schematic of semiconductor QCA by Lent and Tougaw [28].

known as critical thickness, t_{cr} . When monolayers of hetero-junctions are deposited, then at a certain point, the layer thickness t becomes greater than critical thickness t_{cr} . At this time, a very thin semiconductor film buckles due to stress of having different lattice structures from those of the material upon which the films are grown. This huge pressure of the newly formed layer forces the inner layer to pop up to relieve stress, which forms the QD. The formation of QD occurs at $t > t_{cr}$. The density of state equation for QD is

$$\rho_{\text{energy}} = 2 \sum_{n_x, n_y, n_z} \delta(E - E_{n_x, n_y, n_z}), \quad (5)$$

where ρ_{energy} is the energy density and is given as $\rho_{\text{energy}} = \frac{d\rho}{dE}$ and E_{n_x, n_y, n_z} is the finite carrier energy.

QDs are fabricated by the following three methods:

- Electron beam lithography
- Molecular beam epitaxy (MBE)
- Metalorganic vapor phase epitaxy

Among these, MBE is the most used technique today. MBE takes place in ultra-high vacuum (10^{-8} Pa) environment. The deposition rate of MBE is typically less than 3000 nm per h [32]. MBE allows epitaxial growth of films. The ultra-high vacuum environment is required for high purity of the grown films. The reflection high-energy electron diffraction method is used to monitor the growth of the crystal layers. QDs are formed by 3D confinements of different bandgap materials. In a semiconductor, in crystallites whose diameter is smaller than the size of its exciton Bohr radius, the excitons are squeezed, leading to electron confinement.

The thickness of each layer down to a single atom layer is controlled by a computer-controlled shutter. In this way, structures of layers of different materials are fabricated. With the help of such control, development of structures where the electrons can be confined in space are achieved, which results in the formation of QDs.

2.1.4 Magnetic QCA

It is observed that magnetic phenomenon is utilized for data storage, whereas electronic phenomenon for information processing. Thus, ferromagnetism is nonvolatile in nature. Power dissipation has become a challenging issue for present CMOS circuits. As a result, logic implementation using nanomagnets are being researched upon [40–42]. This is because of the following two major advantages of nanomagnet logic:

- i. The nonvolatile nature results in zero standby power dissipation.
- ii. Switching energy of magnetic devices is much less compared to CMOS gates [41].

Nanomagnets are nanoscale magnets that have single magnetization state, viz. up ($\uparrow$) or down ($\downarrow$). Such nanomagnets have size scales of tens to hundreds of nanometers. This is because if the length is too large, the magnetization state will break up into multiple internal domains, whereas if the length is too small, the magnetization state can be switched by random thermal fluctuations and will no longer be stable.

The array of nanomagnets can be placed in either antiferromagnetic ($\uparrow\downarrow$) or ferromagnetic ($\rightarrow\rightarrow$) positions [41]; here, the arrow denotes the direction of the poles of the magnets. It is observed that in the antiferromagnetic position, the direction of the poles gets reversed.

Porod et al. [41] have designed a QCA system using nanomagnets. This kind of logic is termed as magnetic QCA or nanomagnetic logic. Hu et al. [41] have termed a single nanomagnet as a magnetic island, and the magnetic islands are fabricated from 30-nm thin film of permalloy using EBL and standard liftoff technique. Here, four major works done in the MQCA domain have been cited. In the magnetic domain, QCA cells are formed by nanosized ferromagnetic materials. Csaba et al. [33] proposed that information can be propagated through an array of magnetic dots due to dot-dot interactions. Depending on the spin of the magnetic dot, the polarization of a MQCA cell can be determined. Csaba et al. [33] show how signal processing and various logic functions can be realized by the interaction between neighboring magnetic dots. In [33], it was shown how nanowire can be realized by proper placement of nanomagnets, shown in Figure 5A. Here, clock (discussed in Section 2.3) is a periodic oscillating external magnetic field (H). It drives the system initially (Figure 5A), then controls the relaxation of the system to ground state. H turns the magnetic moments of all nanomagnets horizontally,

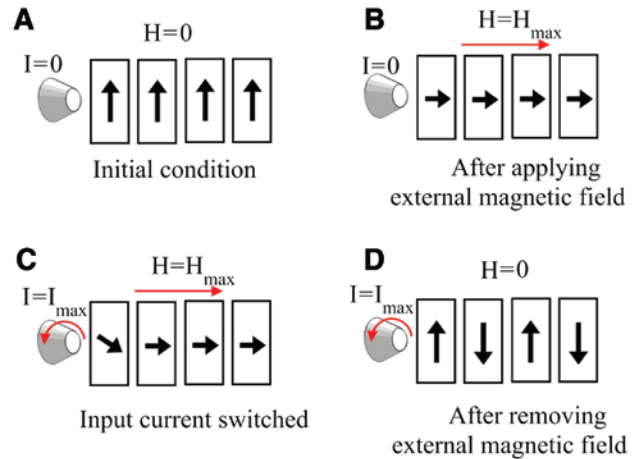


Figure 5: Operating principles of MQCA.

as shown in Figure 5A. When H is removed, i.e. $H=0$, the nano magnets relax into an antiferromagnetic order (shown in Figure 5D). Clocking system is done by induced magnetic field created by applying current (I) [33–37].

Latter in 2004, magnetic cellular automata was proposed by Parish and Forshaw [38] based on the principle of data storage using nanomagnets. One of the advantages of MQCA is that it can be operated at room temperature. Bernstein et al. [39] carried an experimental demonstration of designing of nanomagnet at room temperature. They also proposed how QCA wire and majority gates can be realized using nanomagnets.

2.1.5 Room temperature fabrication of QCA

Very recently, Dilabio et al. [43] have experimentally fabricated QCA cell at 293 K. This invention is expected to remove the major obstacle for QCA realization in room temperature. The QCA device has been fabricated by spatially controlled formation of dangling bonds (DBs) over silicon surface $\langle 100 \rangle$. The silicon atom in the surface shared three bonds with other silicon atom. The unshared atom is bonded with hydrogen atom to form a DB. Each DB has a separation of one atom. Finally, additional electron has been provided inside the DB such that there exists at least one unoccupied DB for each additional electron. Such a cell has a “self-biasing” effect. The binary state of the cell is electrostatically controlled. The most important feature is that the device operates at room temperature (293 K) and largely immune to stray electrostatic perturbation [43].

2.2 QCA basic gates

2.2.1 Majority voter

In QCA technology, data transfer as well as computation operations take place with the help of columbic interactions. There is no concept of charge transfer through wire, like traditional CMOS technology. This is because of the fact that charges remain confined in the QCA cell and ideally do not dissipate. Here, the concept of polarizations comes in, which means that the placement of QCA cells is the a particular manner is required to design any QCA logic gates or QCA wire. The fundamental QCA logic circuit is majority voter (MV) gate. MV is a logic gate whose output is the state of the majority of the inputs [10, 19, 20]. Eq. (6) gives the logic function of a three-input MV, where A, B, and C are the three inputs.

$$MV(A, B, C) = AB + BC + CA \quad (6)$$

The QCA layout of the MV gate is shown in Figure 6a. From the figure, it is seen that there are three input cells, viz. A, B, and C, and one output cell M. Apart from these three cells, there is another cell in the middle. This cell is known as a device cell. The input cells may have different polarizations, i.e. +1 or -1. But as there are three of them, there will always be either two +1 or two -1 polarizations or, in other words, majority of any one of the polarizations will be seen at any point of time. The device cell will simply attain the polarization that is in excess in the input cells. Finally, the output cell will simply reflect the polarization of the device cell due to columbic effect. This is the fundamental operation of the QCA MV gate. The block diagram of an MV gate is also shown in Figure 6b. MV can be used to perform AND as well as OR operations by making one of the inputs, say C, fixed to logic 0, i.e. polarization -1, also known as fixed polarization, and as an OR gate by making one of the inputs fixed to logic 1, i.e. polarization +1 as

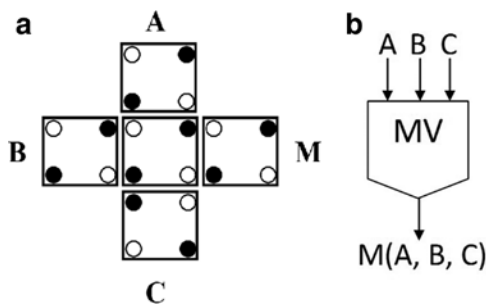


Figure 6: Majority voter circuit. (a) QCA layout; (b) its block diagram.

$$MV(A, B, C) = AB + BC + CA$$

$$MV(A, B, 0) = AB$$

$$MV(A, B, 1) = AB + B + A = A + B$$

2.2.2 QCA Inverter or NOT

Another interesting QCA gate is the QCA inverter. Until now, we are familiar of the fact that any logic operation or data transfer in QCA technology is basically driven by Columbic interaction between the electrons of adjacent QCA cells. The same principle holds true in the case of designing QCA inverters. The basic idea is to have cell(s) at the corner(s) of the output cell. The first figure in Figure 7A shows that the output cell X' has cell at one of its corners. This kind of orientation will force the output cell to attain the polarization opposite of that of the corner cell. A similar operation takes place in the second figure in Figure 7A, but in this case, the output cell has cells in both of its corners. The only difference in this layout is that it will attain a much stable output. For example, in this case, the corner cells are in +1 polarization, so the output cell can never be in +1 polarization due to Columbic interaction and thus will be forced to be in -1 polarization. Two standard cells in a diagonal orientation are designed as QCA inverter. Two types of designs can be possible for QCA inverter or NOT gate. The QCA layout of these inverters is shown in Figure 7A. Also, its logic symbol is shown in Figure 7B.

2.2.3 QCA tile structure

The defect in QCA structures depends highly on the placement of the QCA cell. There are two types of placement defect in QCA structures, viz. misplaced cell defects and missing cell defects. In the first case, the cell might be wrongly fabricated in a misaligned manner, whereas in the second case, the cell might not be fabricated at all. In both cases, the output will be erroneous. In order to cope up with the misplaced/missing cell defect of QCA

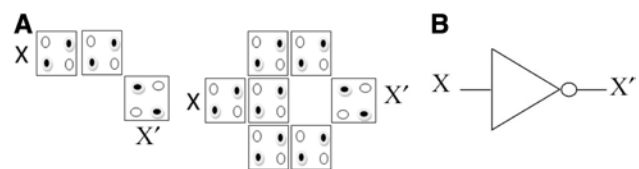


Figure 7: Inverter/NOT circuit. (A) QCA layout; (B) its logic symbol.

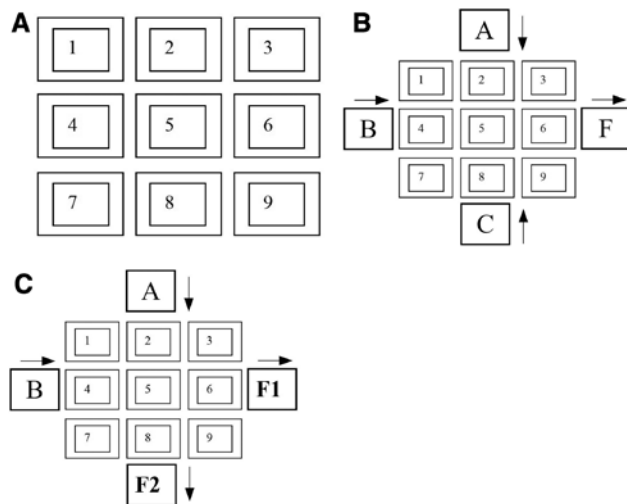


Figure 8: QCA tile structure. (A) Grid representation of 3×3 tile. (B) Block diagram of MV circuit using 3×3 orthogonal tile. (C) A 3×3 baseline tile showing coplanar crossing.

cells, QCA tile structure was proposed by Das and De in their paper [44]. Here, a number of QCA cells are placed closely packed with each other; thus, the probable error of misplacement can be rectified to a large extent. Among various tile structures, the 3×3 tile is found to be most popular because of its versatility. In Figure 8A, a grid representation of the 3×3 tile is presented. It has a total of nine positions for cell placement. The positions for cell placement are marked from 1 to 9. A 3×3 tile-based MV is much more stable and fault tolerant than ordinary three-input MV, as discussed in Section 2.2.1 for the presence of diagonal cells (1, 3, 7, and 9) [44] and the radius effect [45]. Having the grid structure for MV will strengthen the output polarization and will make it more stable. Further, if any of the cell gets misplaced or missing, the adjacent cells of the grid will cope up for it. In this way, the placement problem can be eliminated. The grid structures are not quite favorable for smaller designs because they will increase the cell count of the design, but in bigger circuits, it will be highly beneficial. A block diagram of an MV circuit using a 3×3 tile is shown in Figure 10B. The tile structure shown in Figure 8B is known as 3×3 orthogonal tile [46]. There is another variety of 3×3 tile that is known as 3×3 baseline tile (shown in Figure 8C). The most significant feature of the 3×3 baseline tile is that it supports coplanar crossing without using rotated cells. From Figure 8C, it is seen that polarization of A passes through F2, whereas polarization of input B passes through F1 without mutual interaction. This tile structure is used to design QCA-based Fredkin gate [46]. The detailed structure of the Fredkin gate is discussed in Section 3.1.1.

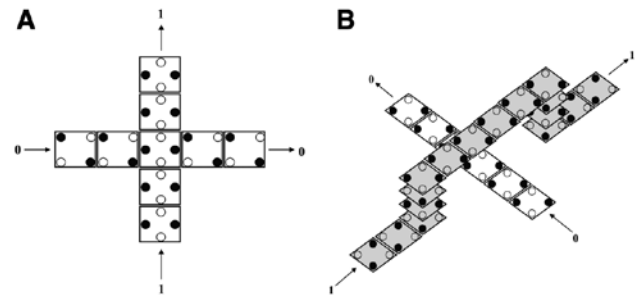


Figure 9: QCA crossovers: (A) coplanar crossover, (B) multilayer crossover.

2.2.4 QCA crossover

Crossover is required to carry data through a QCA wire without affecting the other data inside the circuit. There are two types of QCA crossovers, viz. single layer, as shown in Figure 9A, and multilayer, as shown in Figure 9B. Single-layer or coplanar crossings use only one layer but require using two types of QCAs, i.e. regular and rotated. The regular cell and the rotated cell do not interact with each other when they are properly placed, so rotated cells can be used for coplanar crossings. The interaction between a regular QCA wire and a rotated QCA wire is very interesting. Consider the QCA layout in Figure 9A; there are two regular QCA cells on both sides of a rotated QCA cell. In this case, the Coulombic effect of both the regular QCA cells will nullify each other. As a result, the interaction will not take place and the polarization of the rotated cell will be affected only by the upper rotated cell. Multilayer crossovers utilize the concept of multilayered conventional integrated circuits. It consists of the main cell layer, via layers and the interconnection layer. In case of multilayer crossover, as shown in Figure 9B, the crossings of the two QCAs do not take place at the same layer. While one of the wires, marked in white in the figure, passes through the base layer, also known as the main cell layer, the other wire, marked in brown in the figure, crosses the previous wire through a different layer above the main cell layer. This new layer is known as the via layer, and there are interconnection layers that connect the via layer with the main cell layer.

2.3 Clocking in QCA circuits

Clocking is required for a QCA circuit to synchronize and for information flow control. If we switch a large array of cells at the same time, then data get stuck because electric field (kink energy) never reaches the ground state. Hence,

error occurs at the output. To overcome this problem, various cell arrays are divided into four clocking zones, i.e. C0, C1, C2 and C3.

- It must follow a particular order, viz. $C0 \rightarrow C1 \rightarrow C2 \rightarrow C3$.
- If the length of any QCA wire is greater than $E_{ij}/k_b T$, then the wire is further partitioned into separate clock zones.

Generally, four multiphase clocking signals of phase lagging of $\pi/2$ are applied, as shown in Figure 10A. This type of clocking system is called the Laundauer type [47]. During a complete cycle, each zone goes through the four phases.

- Switch phase: The QCA cell starts to move from an unpolarized state to a polarized state and the barriers of the dots are raised. The electrons start tunneling through dots as the dots are influenced by the electron of its neighbor cell.
- Hold phase: The barrier of the cell is in the high value, electrons cannot tunnel through dots, and cells maintain their current states, i.e. fixed polarization.
- Release phase: The barrier is lowered, electrons can tunnel through dots, and states of the cell become unpolarized.
- Relax phase: The barrier remains lowered and cells stay in the unpolarized state.

Also, Lent et al. proposed another type of clocking signals for reversible circuit, which is Bennett-type clocking [47, 48]. The waveform of Bennett clocking is shown in Figure 12B. The principle of this clocking is to first compute the results by latching the cell array from input to output and then uncomputing by latching array to relax to an unpolarized state from output to input. From Figure 10A and B, we see that Bennett clocking requires more than twice the number of clock fractions than does the Laundauer clocking scheme [48].

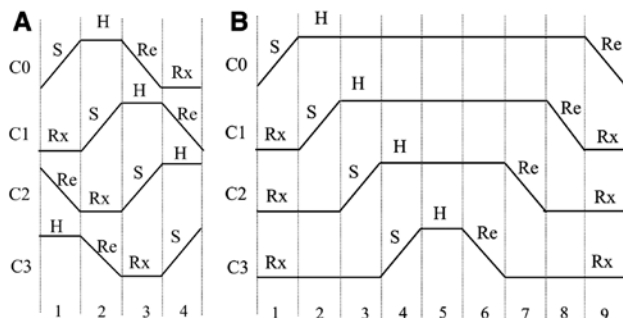
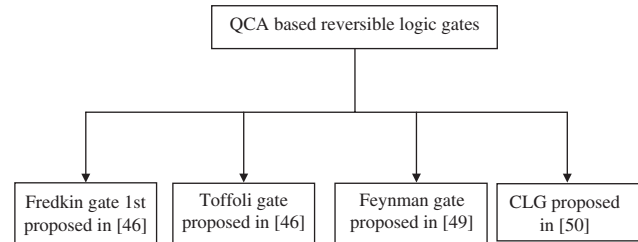


Figure 10: Clocking used in QCA circuit. (A) Laundauer clocking waveform, (B) Bennett clocking waveform. S, switch phase; H, hold phase; Re, release phase; Rx, relax phase.

3 Reversible computation in QCA

In 1993, Lent et al. introduced reversibility in QCA-based circuit design [10]. In the following years, several authors have proposed several reversible gates in QCA. In the chart given below, some of the important designs of reversible logic gates based on QCA are highlighted. All these designs are further modified and proposed in latter work.



3.1 Basic reversible logic gates

In this section, we will discuss various reversible gates that have been proposed in QCA.

3.1.1 Fredkin gate

One of the most used reversible logic gates is the Fredkin gate, or controlled SWAP gate. It is a 3×3 reversible gate. If A, B, and C are the inputs, then P, Q, and R will be the outputs such that $P=A$, $Q=\bar{A}B+AC$, and $R=\bar{A}C+AB$. This will be clear by the truth table of the Fredkin gate in Table 1.

From the truth table, it is observed that outputs Q and R will reflect the inputs B and C when input A is 0. But when A becomes 1, swapping will take place, i.e. the output Q will reflect input C and output R will reflect input B. From this truth table, the change in entropy (ΔH)

Table 1: Truth table of the Fredkin gate.

Input			Output		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

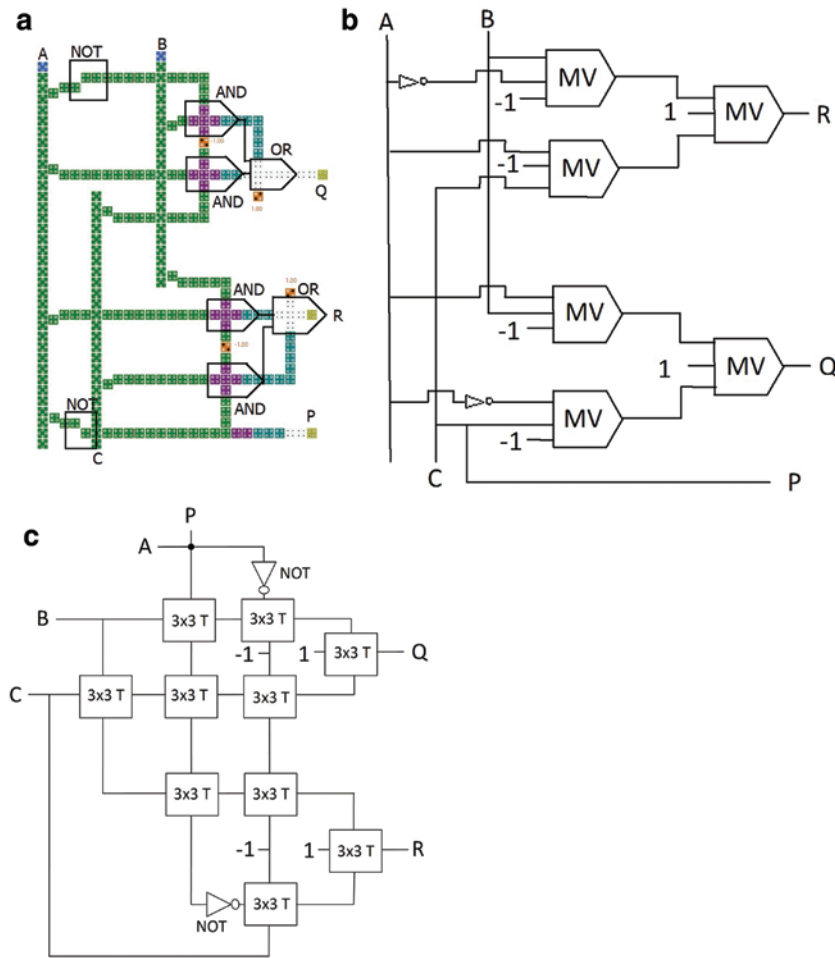


Figure 11: A QCA-based Fredkin gate circuit as proposed by (a) Ma et al. [49], (b) Thapliyal and Ranganathan [50], and (c) Das and De [46] (3×3 T: 3×3 tile-based MV).

by calculating H_{in} and H_{out} is calculated. It is found that $H_{in} = H_{out} = -8 \cdot \frac{1}{8} \ln\left(\frac{1}{8}\right)$ and $\Delta H = H_{in} - H_{out} = 0$. So energy dissipation is $\Delta E = k_B T \ln 2 \cdot (\Delta H) = 0$. Ma et al. [49] was the first to design a QCA-based Fredkin gate; the QCA layout of the circuit is shown in Figure 11a. In Figure 11a, A, B, C are the inputs and P, Q, R are the outputs. The layout is analyzed using the following equations:

$MV3(A, C, -1) = AC$; MV3 is the three-input MV, $-1 = -1$ fixed polarization at the third input. In Section 2.2.1, we have discussed how MV can be used to design AND and OR gates.

$$Q = MV3(MV3_1, MV3_2, 1)$$

$$MV3(A, B, -1) = AB$$

$$MV3(\bar{A}, C, -1) = \bar{A}C$$

$$R = MV3(MV3, MV3, 1)$$

$$P = R$$

They use coplanar crossing in their design, so cell count is reduced to a large extent. Moreover, the output of

the Fredkin gate can be obtained in one clock cycle delay. But the design uses four extra ancilla inputs. These bits are destroyed, so actual heat dissipation is $4k_B T \ln 2$ J. Also, the number of the fan-out is 8.

In the same year, in 2009, another paper was published by Thapliyal and Ranganathan [50], where the design approach of the QCA-based Fredkin gate is basically same as in [49], shown in Figure 11b. Their design used six extra ancilla inputs. These bits are destroyed, so actual heat dissipation is $6k_B T \ln 2$ J. Also, the number of fan-out is 6.

In 2010, another significant modification of the QCA-based Fredkin gate design was reported by Das and De [46]. The Fredkin gate proposed [46] is based on the QCA 3×3 orthogonal and baseline tile structure. The tile structure helps in implementing versatile logic functions and is highly area efficient. The proposed Fredkin gate QCA layout is given in Figure 11c. The circuit has four extra ancilla inputs, which is equivalent to heat dissipation of

Table 2: Truth table of the Toffoli gate.

Input			Output		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

$4k_B T \ln 2$ J and six fan-outs. In Figure 11c, a 3×3 orthogonal tile structure is used as majority gates, whereas a 3×3 baseline tile is used for coplanar crossover. The majority equation of this design is same as of the other two.

3.1.2 Toffoli gate

The Toffoli gate is also a 3×3 reversible gate. The truth table of the Toffoli gate is given in Table 2, which gives the logical expressions for outputs as $P=A$, $R=C$, and $Q=\overline{AB+B(A \oplus C)}$. Here, it is found $\Delta H=0$; i.e. energy dissipation is asymptotically zero. The Toffoli gate is known as controlled NOT gate because the output R will be the inverse of input C when both inputs A and B are 1. The QCA-based circuit of Toffoli gate was also first proposed by Ma et al. [49], which is shown in Figure 12. It has two extra ancilla inputs, equivalent to heat dissipation $2k_B T \ln 2$ J and six fan-outs. The majority equation for Figure 12 is shown below:

$$P=A$$

$$R=C$$

$$MV(\overline{B}, A, -1) = \overline{B}A$$

$$MV(\overline{C}, \overline{A}, 1) = \overline{C} + \overline{A}$$

$$MV(A, B, C) = AB + BC + CA$$

$$Q = MV(MV(\overline{B}, A, -1), MV((\overline{C}, \overline{A}, 1), MV(A, B, C)))$$

$$= MV(\overline{AB}, \overline{A} + \overline{C}, AB + BC + CA)$$

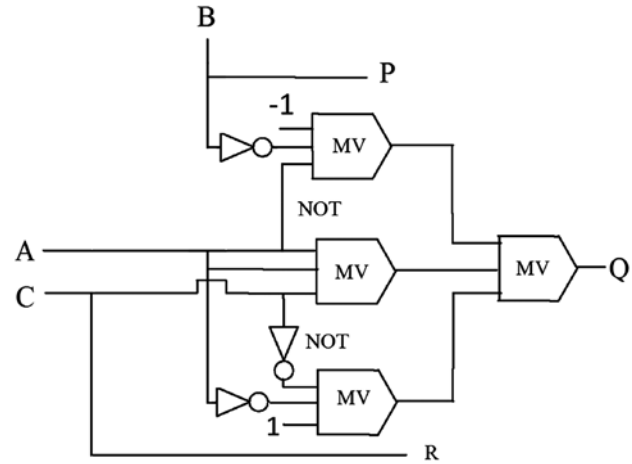
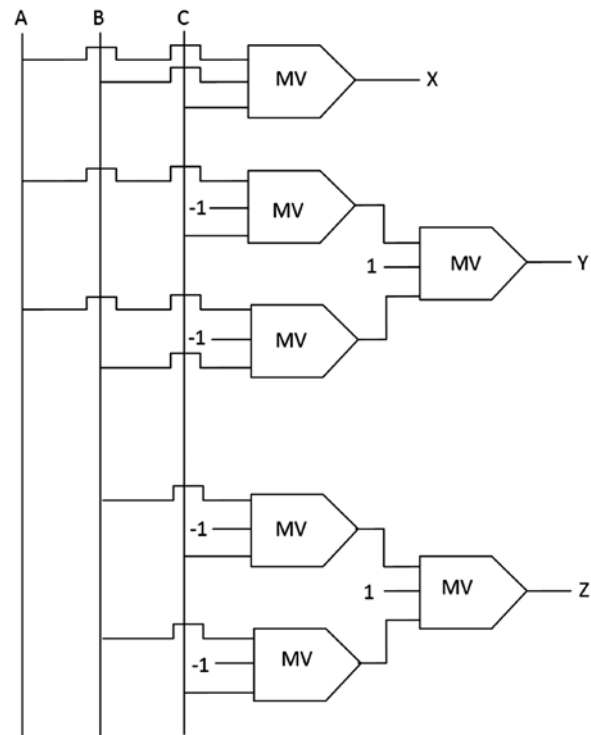
$$= \overline{AB} \overline{C} + \overline{AB} C + A \overline{B} C + \overline{A} B C$$

$$= \overline{AB} + \overline{B} A C + B A \overline{C}$$

$$= \overline{AB} + B(A \oplus C)$$

3.1.3 Reversible universal gate

Sen et al. [51] proposed the reversible universal gate (RUG), which is shown in Figure 13. The logical expressions of the outputs are as follows:

**Figure 12:** Schematic diagram of the Toffoli gate proposed by Ma et al. [49].**Figure 13:** Schematic diagram of the RUG gate proposed by Sen et al. [51].

$$X = M(A, B, C)$$

$$= AB + BC + CA$$

$$Y = MV[MV(A, C, -1), MV(A, B, -1), 1]$$

$$= AB + AC$$

$$Z = MV[MV(B, C, -1), MV(C, B, -1), 1]$$

$$= BC.$$

It has six extra ancilla inputs, equivalent to heat dissipation $6k_B T \ln 2$ J and eight fan-outs.

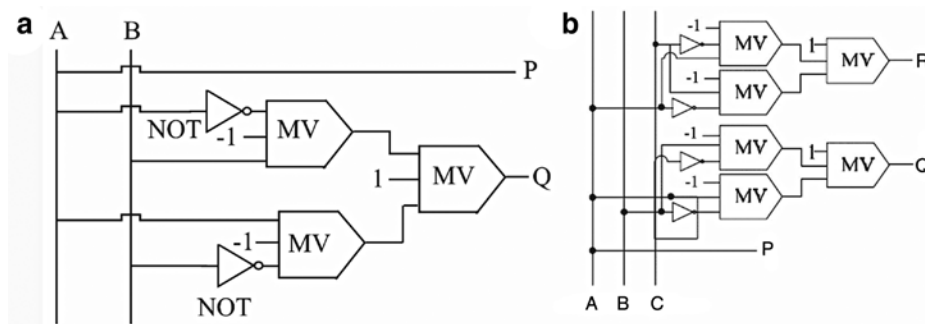


Figure 14: Schematic diagram of (a) FyG and (b) double FyG proposed by Bahar et al. [53].

3.1.4 Feynman gate

The FyG is a 2×2 reversible logic gate. The logical expression of two outputs are $P=A$ and $Q=A \oplus B$, where A and B are two inputs. If $B=0$, then $Q=A \oplus 0=A$; i.e. it copies the inputs into two without crating fan-out and bit erase. Hence, this reversible gate reduced fan-out. In [52], Thapliyal and Ranganathan have proposed a QCA-based FyG. The schematic diagram of QCA layout of a FyG is shown in Figure 14a. Here, it is seen that there are three extra ancilla inputs in the circuit, which is equivalent to heat dissipation $3k_B T \ln 2$ J as these bits are lost during operation. Also the number of fan-out is three.

In [53], Bahar et al. proposed a modification on the FyG. The authors proposed a QCA-based double FyG. The double FyG is a 3×3 structure with A, B, and C as inputs and P, Q, and R as outputs such that $P=A$, $Q=A \oplus B$, and $R=A \oplus C$.

The truth table of the double FyG proposed in [53] is given in Table 3. It is seen from the truth table that the input combination is uniquely represented at the output, which supports the reversibility of the proposed gate. Here, it has also been found that $\Delta H=0$, and Figure 14b shows that there are six extra ancilla inputs in the circuit, which is equivalent to heat dissipation $6k_B T \ln 2$ J as these bits are lost during operation.

Table 3: Truth table of the double FyG.

Input			Output		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

3.1.5 CQCA gate

The CQCA gate was proposed by Thapliyal and Ranganathan [50]. The schematic diagram of the proposed CQCA gate is shown in Figure 15. The proposed CQCA gate performs the output logic expressions, $P=A$, $Q=AB+BC+CA$, and $R=\bar{A}B+BC+\bar{A}\bar{C}$. CQCA is a conservative logic gate. The circuit has no ancilla inputs and also $\Delta H=0$; hence, theoretically, it does not dissipate energy. The number of fan-out is four.

3.1.6 CLG gate

Another 3×3 conservative logic gate with reversible property was proposed by Das and De [46]. The logic expression of CLG is $P=C$, $Q=AB+BC+CA$, $R=\bar{C}B+AB+\bar{C}A$. This is basically a similar type of CQCA gate. The QCA circuit of the CLG gate is shown in Figure 16. Here, they used 3×3 tile-based MV gates. CLG has both bit preservation as well

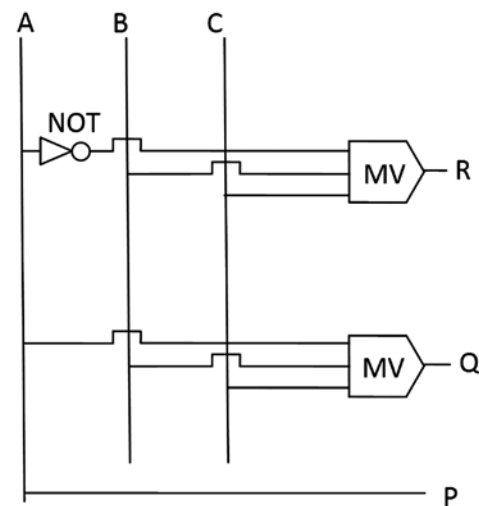


Figure 15: Schematic diagram of the reversible CQCA gate proposed by Thapliyal and Ranganathan [50].

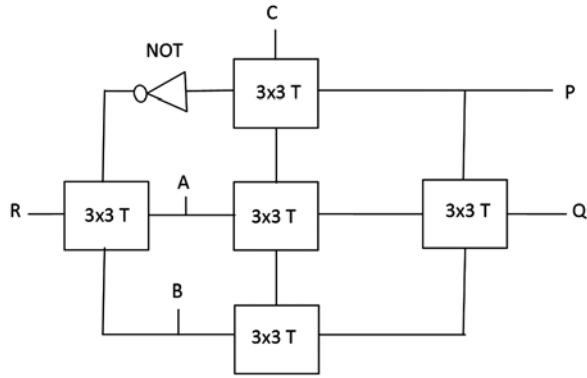


Figure 16: Schematic QCA layout of the CLG gate proposed by Das and De [46]. 3×3 T: 3×3 tile-based MV.

as parity preservation properties. As a result, CLG can be used as both reversible and conservative logic. Due to the use of tile structure, the design can be achieved in a single layer; also, the stability of the output is much higher. Here, no ancilla inputs occurred, no bit loss happens, and also $\Delta H=0$. So, theoretically, it does not dissipate energy, but the circuit has three fan-outs.

3.2 Complex reversible logic circuit design using basic reversible logic gates

3.2.1 Reversible full adder

Any complex circuit designed with basic reversible gates are also reversible in nature. Bruce et al. [6] designed a full-adder circuit using four Fredkin gates as shown in Figure 17. Total ancilla inputs are two and the number of garbage outputs is three.

Here, from the logical expressions of Fredkin gate, the logical expressions of the different outputs can be written as

$$\begin{aligned} P1 &= X_i, Q1 = X_i, R1 = \bar{X}_i \\ Q2 &= \bar{Y}_i Q1 + Y_i R1 = \bar{Y}_i X_i + Y_i \bar{X}_i = X_i \oplus Y_i, \\ R2 &= \bar{Y}_i R1 + Y_i Q1 = \bar{Y}_i \bar{X}_i + Y_i X_i = \bar{X}_i \oplus Y_i, P3 = Q2 = X_i \oplus Y_i, P4 = C_i \\ C_{i+1} &= Q2 \cdot P1 + Q2 \cdot P4 = Q2 \cdot P1 + Q2 \cdot C_i = (X_i \oplus Y_i) X_i + (X_i \oplus Y_i) C_i \\ &= X_i Y_i + (X_i \oplus Y_i) C_i S_i = C_i \cdot P3 + C_i \cdot R2 = C_i (X_i \oplus Y_i) + C_i (X_i \oplus Y_i) \\ &= (X_i \oplus Y_i \oplus C_i) \end{aligned}$$

3.2.2 Reversible latches

Thapliyal and Ranganathan proposed the reversible D latch and J-K latch using Fredkin gates in their article

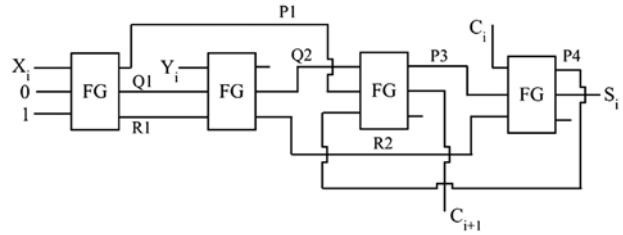


Figure 17: Reversible full-adder circuit proposed by Bruce et al. [6]. FG, Fredkin gate.

[54]. In Figure 18A and B, the block diagrams D latch and J-K latch are shown respectively. The characteristic equations of such latches are $Q_{D-latch} = DE + \bar{E}D$ and $Q_{JK-latch} = (J\bar{Q} + \bar{K}Q)E + \bar{E}Q$ [54]. The D latch has two garbage outputs and the J-K latch has seven garbage outputs and four Ancilla inputs.

3.2.3 Reversible CED circuit

Thapliyal and Ranganathan used FyG to design a reversible comparator for concurrent error detection (CED), where the authors used FyG to avoid the fan-out constraints [52]. The schematic block diagram of CED is shown in Figure 19. Here, R is a reversible gate that maps input vector X to output vector Y and $\bar{R}$ is the inverse reversible gate of R , which maps input vector Y to output vector X . Now, if R and $\bar{R}$ are cascaded together, the input vector can go back at the end. Thus, by comparing the original input vector with the regenerated ones, any error that occurred can be analyzed. Here, the authors have cascaded R with $\bar{R}$ and the garbage outputs of R are directly passed as the inputs of $\bar{R}$, whereas each primary output of R is passed through a FyG, with its second input being 0. As shown in Figure 19, the primary output Y_k is passed through FyG. As a result, two copies of the primary outputs are obtained, one of which is passed to the input of $\bar{R}$ to perform CED. Finally, the original input vector and the regenerated input vector are passed through a comparator to generate the error signal.

4 Comparative study

In this section, we present a comparative study of all the different QCA-based reversible logic gate designs that have been highlighted in Section 3. The comparison of the QCA circuits is done on the basis of cell count, number of MVs, area, number of layers used, clock cycles, and

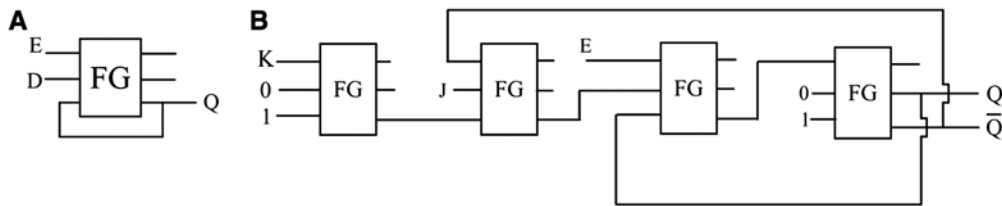


Figure 18: Reversible latches. (A) Reversible D-latch and (B) reversible JK-latch proposed by Thapliyal and Ranganathan [54]. FG, Fredkin gate.

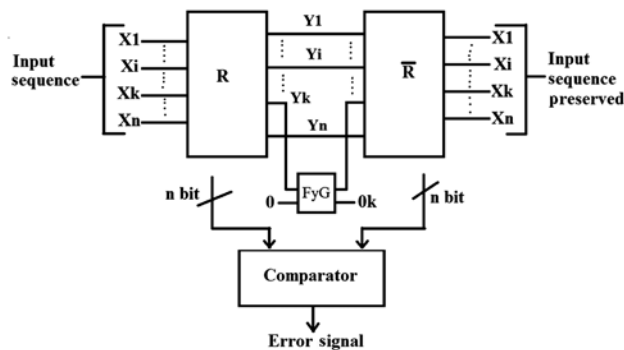


Figure 19: Block diagram of the error detection scheme proposed by Thapliyal and Ranganathan [52].

Table 4: Comparative analysis of the QCA-based Fredkin gate proposed in [49] and [46].

Proposed by	Cell count	MVs	Area	Layer	Latency	Key design aspect
Ma et al. [49]	185	6	0.54 μm^2	1	One clock cycle (four clock zones)	Use of both 90° and 45° cells
Das and De [46]	246	6	0.33 μm^2	1	One clock cycle (four clock zones)	Use of 3×3 orthogonal tile

latency. In Table 4, the comparative studies of the two types of the design of Fredkin gate that are proposed in [49] and [46], respectively, are presented. From Table 4, it

Table 5: Comparative analysis of the QCA-based Toffoli gate proposed in [49] and RUG proposed in [51].

Proposed by	Cell count	MVs	Area	Layer	Latency	Key design aspect
Ma et al. [49]	167	4	0.558 μm^2	1	1 clock cycle (four clock zones)	Use of both 90° and 45° cells
Sen et al. [51].	≈298	7	–	1	1.75 clock cycles (seven clock zones)	Use of both 90° and 45° cells

is observed that by using QCA tile structure as discussed in Section 2.2.3, the area of the circuit can be significantly reduced, although the cell count gets higher to some extent, whereas the other factors, like number of layers and latency, remain the same. Another interesting factor that can be observed from Table 4 is that the tile structure uses only 90° cells; thus, it is much more stable in comparison to the other design [42].

Next, in Table 5, a comparison between the Toffoli gate proposed by Ma et al. [49] and RUG proposed by Sen et al. [51] are shown. The reason we chose to compare these two designs is that both are similar designs and RUG is actually a modified version of the Toffoli gate.

Table 6 provides a comparative analysis of three new reversible gates designed in QCA. These are the double FyG proposed in [53], the CQCA gate proposed in [50], and the CLG gate proposed in [46]. Among all the designs, the

Table 6: Comparative analysis of the QCA-based double FyG proposed in [53], CQCA proposed in [50], and CLG proposed in [46].

Proposed by	Gate proposed	Cell count	MVs	Area	Layer	Latency	Key design aspect
Bahar et al. [53]	Double FyG	51 for type 1 and 96 for type 2	6	0.06 μm^2 for type 1 and 0.094 μm^2 for type 2	1	0.5 clock cycle (two clock zones) for type 1 and 0.75 clock cycle (three clock zones) for type 2	Single layer design by using only 90° cells
Thapliyal and Ranganathan [50]	CQCA	117	2	0.11 μm^2	1	0.5 clock cycle (two clock zones)	Use of both 90° and 45° cells
Das and De [46]	CLG	94	3	0.11 μm^2	1	0.5 clock cycle (2 clock zones)	Use of both 90° and 45° cells

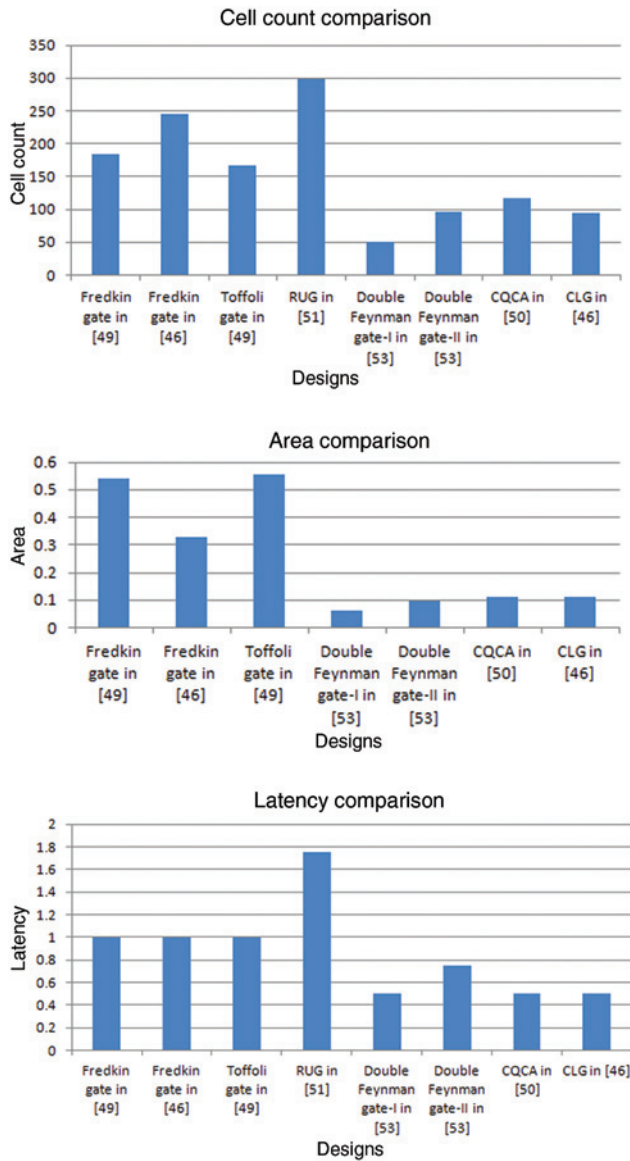


Figure 20: Comparison of (A) cell count, (B) area, and (C) latency of different QCA-based reversible gates.

CLG design has both cell count, area, and latency benefits because it has the same latency and also a coplanar design, but cell count and MV count are less compared to other designs. Thus, CLG is beneficial to use in various complex QCA-based reversible logic designs.

In Figure 20A, B, and C, the cell count, area and latency of the various QCA-based reversible gates discussed in Section 3 are shown graphically.

In general, evaluation of the RLGs can be comprehended easily with the help of one main factor, which is circuit complexity. This parameter can be obtained by counting the number of logical calculations (T) [55, 56], which is shown in Table 7. Here we consider

Table 7: Complexity of different reversible logic gates.

Reversible logic gate	Number of inputs/outputs	Total logical calculations
Fredkin gate (FG)	3	$2\alpha+4\beta+2\delta$
Toffoli gate (TG)	3	$\alpha+\beta$
RUG	3	$5\alpha+10\beta$
FyG	2	α
Double FyG (Fy2G)	3	2α
CQCA	3	$5\alpha+9\beta+3\delta$
CLG	3	$5\alpha+9\beta+3\delta$

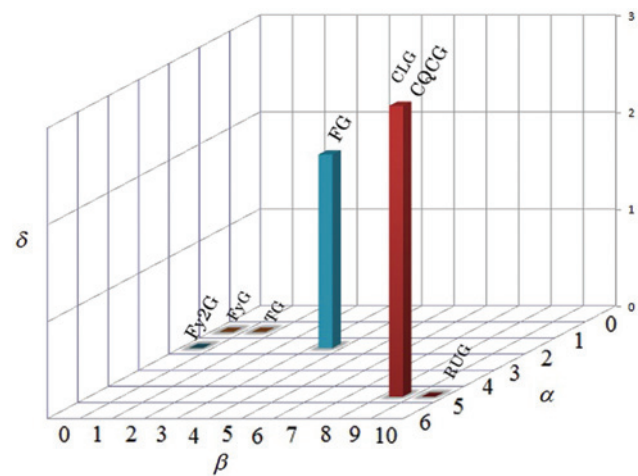


Figure 21: Different gate number (α, β, δ) variations for different reversible logic gates.

α =a two-input EXOR gate calculation

β =a two-input AND gate calculation

δ =a NOT gate calculation

If we plot the three parameters α, β , and δ in Figure 21, we can easily say that the CLG or CQCA gate has more logical calculations and FyG has less. Also, SCL complexity is twice the TG. According to the complexity order, we can write, $RUG > CQCA = CLG > TG > Fy2G > FyG$.

5 Conclusion

This paper presents review work on various reversible logic gates that have been designed in the QCA paradigm. QCA is one of the most promising candidates of post-CMOS design. Various techniques by which QCA cells have been fabricated are shown in this paper. Although it is not possible to fabricate all of the QCA cells in room temperature, magnetic and semiconductor QCA cells are successfully

fabricated in room temperature. The fabrication process has been described. Different variations in the design done on basic reversible gates like the Fredkin gate, Toffoli gate, and FyG are studied. Also, some of the modifications done on earlier gates as well as some new reversible gates that have been proposed in latter literature are highlighted. By the comparative study, major variations in the cell count of the different QCA-based reversible gates have been observed. However, the latencies of all the designs discussed in this paper are more or less equal.

Acknowledgments: T. Purkayastha and D. De are grateful to The University Grants Commission, India, for providing with the grant for accomplishment of the project under the UGC Major Project File No. 41-631/2012(SR).

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