Review

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State of the art of metal oxide memristor devices

Abstract: Memristors are one of the emerging technologies that can potentially replace state-of-the-art integrated electronic devices for advanced computing and digital and analog circuit applications including neuromorphic networks. Over the past few years, research and development mostly focused on revolutionizing the metal oxide materials, which are used as core components of the popular metal-insulator-metal memristors owing to their highly recognized resistive switching behavior. This paper outlines the recent advancements and characteristics of such memristive devices, with a special focus on (i) their established resistive switching mechanisms and (ii) the key challenges associated with their fabrication processes including the impeding criteria of material adaptation for the electrode, capping, and insulator component layers. Potential applications and an outlook into future development of metal oxide memristive devices are also outlined.

**Keywords:** memory technology; memristor; RRAM; thin film.

1 Introduction

Progress in the field of semiconductor electronics continues to have profound influence on human society. In particular, this has led to an unprecedented growth in the information communication technology field, as well as virtually every other field of engineering and technology. Hence, the demand for faster and more efficient information processing systems continues to increase at a high rate. Typical trending is primarily driven by the quest to create a ubiquitously connected world and the realization of the internet of things. Since the establishment of Moore's law in the 1960s, device evolution can be mainly traced by incessant micro-sizing to reach higher processing speed and to facilitate the production of sizeable packing densities at lower fabrication costs. Particularly, "memory" constitutes nowadays more than 60% of the modern processor area, which makes it a major target for device miniaturization. Microprocessors today provide unmatched computing power owing to state-of-the-art complementary metal-oxide-semiconductor (CMOS) technology, which ultimately enables the so-called "non-volatile memory". Nonetheless, further projection of the current CMOS design to satisfy the growing needs for higher processing capacity and larger data size while miniaturizing device scale has now reached its practical limits. Key challenges arise from extending the performance capstone of actual devices in terms of leakage current, power consumption, and switching speed, when the main constraint is often attributed to structure, outside the peculiar capabilities of the CMOS material itself [1]. Hence, technological breakthroughs pushing forward novel device configurations are highly desirable to achieve new scalable platforms that would outperform the classic CMOS design. Nowadays, researchers in the field of micro or nano electronics are focusing their attention on "memristor" technology as a viable alternative to early CMOS-based approach for device miniaturization. The concept of a "memristor" (or memory-resistor) device was initially interpreted by Leon Chua in 1971, as the fourth fundamental circuit element based on symmetry arguments [2–4]. The device was proposed as a missing passive element that could link the magnetic flux to the electric charge, a property that cannot be obtained by any combination of the other three fundamental elements, namely, the resistor, the capacitor, and the inductor. An elementary memristor can be perceived as a two-terminal device with a sandwiched metal/insulator/metal (MIM) structure, which is generally integrated in an elementary crossbar circuit, as illustrated in Figure 1. Typical configuration allows for smaller interconnection and higher composite density than the one achieved using conventional three-terminal transistors [5]. Another

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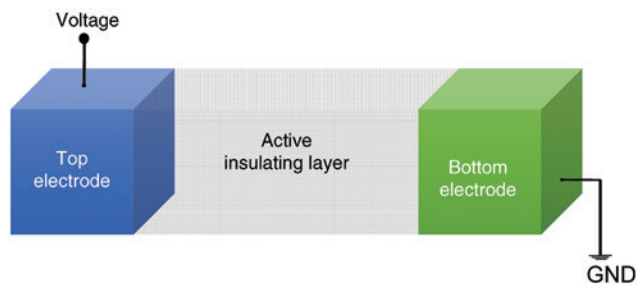
Figure 1: Schematic of memristor device structure with metal/insulator/metal (MIM) configuration.

peculiar feature of a memristor is its memory function, which originates from a resistance state that the device remembers after being subjected to an electric potential difference over a certain time. Although the theory of memristive switching was introduced 40 years ago [3, 4], interpretation of the driving mechanism only appeared two decades later and remains obscure to date [6]. The first clear connection between Chua's theory and the practical demonstration of a memristor device was achieved by Hewlett-Packard Labs in 2008, when scientists observed a memristive behavior at the nanoscale level using thin-film titanium dioxide as insulator layer [5]. With a simple mathematical model, researchers at HP Labs were further able to demonstrate that the memristance phenomenon arises naturally in nanoscale systems. HP prototype memristors have been shown to store data, process logic at nanoscale footprint, exhibit long retention time, and offer fast, non-volatile, and low-power electrical switching [1, 5]. Memristors continue to stir up a continuous worldwide research market growth as promising alternatives to classic CMOS devices, owing to their potential scalability and low power consumption for memory applications. While interest in memristive devices is steeply increasing (Figure 2), successful commercialization of this technology requires

Figure 2: Cumulative publication per year from 2008 to 2014. The number of publications is obtained by searching the following keywords: memristor, RRAM, and resistive switching from the header "Topic" of the Web of Science electronic site https://webof-knowledge.com/.

robust and predictive understanding of its fundamental mechanisms [7]. Impeding difficulties on correlating basic mathematical models with performance data collected out of physical devices are viewed as the main barrier for practical implementation of memristors in a wide variety of applications. One of the most complicated processes to understand and control at the molecular view is the electrical switching mechanism as a function of physical core parameters including (i) the chemistry of materials and (ii) the commonly neglected stochastic and interfacial phenomena arising between the sandwiched layers of the device upon physical contact or during electrical operation [1]. Access to such contained information to provide better description of the mechanistic operation of physical memristor devices would hence require thorough investigations of the physico-chemical properties of the materials configured down to nanoscale levels.

Hence, this review article aims to present an overview of the recognized ion-transport resistive switching mechanism in metal oxide memristors. Focus is placed on distinguishing between the physical and chemical processes that underlie the functionality of anionic and cationic devices, to explain the bipolar and unipolar switching behavior observed in each case. The review also aims to provide a description of existing device configurations to highlight the implication of bulk and interfacial properties of the elementary device materials onto the overall memristive performance characteristics. The mapping covers the physical and chemical angle to provide guidance on the selection criteria of key components involving electrodes, capping, and switching metal oxide materials, including fabrication processes for the purpose of device-design optimization. The review concludes with various potential applications anticipated for metal oxide memristors, with an outlook on the pending challenges observed on their integration into the semiconductor market.
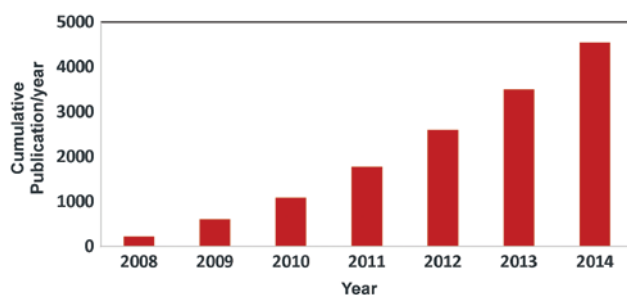
2 Switching mechanism

The first switching mechanisms were elucidated in the late 1990s with a wide variety of oxide systems [7–10]. Nowadays, common studies depict the memristive switching behavior based on a popular thin-film MIM configuration, where the insulator layer is composed of one or more metal oxides with semiconducting properties [7]. To act as memristor, a physical MIM device must exhibit a range of internal resistive states, which are tunable in a quasi-stable manner. Different factors play a key role on defining the instantaneous resistive state of the device, of which the applied electric

field and the compliance current can be externally manipulated during device characterization. Other restricted synergistic determinants, including (i) electron mobility, (ii) gradient of species concentrations, and (iii) gradient of temperature within the insulator region, closely depend on the solid-state properties of the semiconducting material (i.e. lattice defects) and hence require the modification of the fabrication process for further tuning.

The commonly asserted model for resistive switching in metal oxide memristors is the formation and rupturing of conductive filaments inside the active layer, which cause the device to shift from the "Off" state to the "On" state and vice versa. The existence of one or more filaments between the two electrode terminals creates a low-resistance state (LRS), while the absence of these filaments generates a high-resistance state (HRS) (Figure 3). Suggested explanations for this model mostly involve two main resistive switching mechanisms: (i) the valence change memory (VCM) and (ii) the electrochemical metallization (ECM) memory. The valence change process particularly builds on induced anion migration that progressively modifies the stoichiometry of the insulator region via oxidation-reduction reactions. The ECM mechanism relies on the oxidative interfacial dissolution of an active metal electrode, followed by subsequent cation migration across an ion-conducting electrolyte layer, acting as an insulator [11]. In some cases, a thermochemical process is also described in addition to these two main mechanisms, to further justify some structural and stoichiometric modification changes in the insulator layer as a result of current-induced thermal effects [12, 13].

2.1 VCM resistive switching mechanism – anionic devices

Evidence of resistive switching was first demonstrated with thin film/metal oxide/metal sandwiches half a century ago
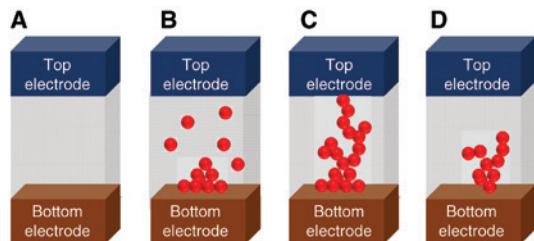
Figure 3: Schematics of resistive switching according to a filamentary conduction model. (A) Native insulator (HRS); (B) creation of conductive channels via electroforming; (C) conductive filaments in a Set process (On state, HRS to LRS transition); and (D) filament rupture in a Reset process (Off state, LRS to HRS transition).

[14, 15]. Considerable effort has been made since to study the switching mechanism in a variety of oxide systems, ranging from simple binary transition metal oxides (e.g. HfO_2, TiO_2, ZnO, Nb_2O_5, Ta_2O_5, MoO, WO, MnO, NiO, and CuO) to perovskites (e.g. $SrTiO_3$, $Ba_{0.7}Sr_{0.3}TiO_3$, $SrZrO_3$, and $BiFeO_3$) and transparent conducting oxides, such as SnO_2 and indium tin oxide (ITO) [10, 16–22]. The fundamental mechanism agreed for switching in these oxides, which are classified as "anionic devices", relies on the migration of oxygen anion species under an external electric field.

In most cases, an electroforming step is required before reproducible device switching can be detected at lower voltage values [22]. The electroforming process (soft or hard) [23] is usually achieved by applying a large electrical bias across the two terminals of the memristor device within a certain time interval, in order to generate initial conductive channels via Joule heating effect. The forming step can be suppressed by appropriately modifying the fabrication process to readily introduce oxygen vacancies in order to facilitate the migration of anions within the switching layer [24].

Understanding the filament formation theory in relation with the external electric field applied and with the local generation of Joule heating is still one of the major complexities to unravel in the valence change model. The following factors are suggested to explain the driving force of anion transport during filament formation: (i) drift by electric potential gradient, (ii) electro-migration assuming an electron kinetic energy, (iii) Fick diffusion due to ion-concentration gradient, and (iv) thermophoresis due to temperature gradient [1]. The valence change pathway in metal oxide memristors is often described by a movement of oxygen species that alters the stoichiometry of insulator sub-lattice, resulting in a concentration gradient of mobile anion species due to parallel vacancy formation in the opposite direction. In most cases, an under-stoichiometric region characterized by several conducting filaments is hence formed, such as the Magnéli phase (M_nO_{2n-1}), which is often reported with titanium dioxide (TiO_2) memristors [25].

In order to modulate the resistive switching in anionic devices, naturally existing or initially formed conductive filaments can be further tuned by controlling the magnitude of external electric field applied [26–28].

2.2 ECM resistive switching mechanism – cationic devices

The ECM mechanism is usually described in MIM devices involving an electrochemically active electrode (AE), such

as Ag or Cu, and a noble counter electrode (CE), such as Pt, Au or W [29–32]. Similar to anionic devices, electrochemical switching in cationic devices is based on filament formation throughout the insulator material acting as solid electrolyte. Conductive channels usually form via the movement of dissolved metal cations from the interface of the electro-chemically active electrode into the insulator region. The need of a forming step is reported as common pre-requirement before observing reproducible resistive switching in several cationic systems. An assumption of structural changes induced in the electrolyte crystal during the forming step is made to explain the creation of conductive filaments via hosting nano template channels that serve as diffusion paths for the migrating metal actions [7, 11, 33–35].

When an external electric field is applied, dissolved metal cations tend to move towards the inert counter electrode, leaving behind metal vacancies. Hence, gradual migration of metal cations decreases the effective thickness of the insulating layer owing to a progressive nucleation and growth of conductive filaments. For example, the following steps subsequently take place when a sufficient positive bias voltage is applied to a Cu electrode (AE), during the forming and Set processes (i.e. from HRS to LRS) of an Al/Cu/GeO$_x$/W memristor [35]:

1. Anodic dissolution of the Cu electrode (half-reaction oxidation process): $Cu \rightarrow Cu^{2+} + 2e-$;
2. Migration of Cu^{2+} ions toward the inert tungsten electrode (CE), driven by external electric field and Joule heating. Ion movement is facilitated along rapid diffusion channels that are created by grain boundaries existing inside the GeO$_x$ semiconducting electrolyte crystal.
3. Reduction and electro-crystallization of Cu^{2+} ions at the interface of the W counter electrode, leading to growth of nano-width Cu filaments (half reaction equation): $Cu^{2+} + 2e- \rightarrow Cu$;

Once the Cu filaments short circuit the GeO$_x$ to create a low-resistance metallic ion trail between AE and CE, the memristor device is switched On from HRS to LRS.

For a Reset process (i.e. from LRS to HRS), a negative voltage is applied to Cu (AE), which leads to dissolution/rupture of existing nano Cu metallic filaments due to oxidation (i.e. reversed redox process) and potential Joule heating effect. Hence, reversing the electrode polarity allows for flipping of the migration of dissolved Cu^{2+} ions back towards Cu (AE).

3 Switching behavior

Two different switching modes, (i) "unipolar" (or nonpolar) and (ii) "bi-polar", are generally recognized for anionic and cationic memristor devices. The schematics of I-V curve characteristic of unipolar and bipolar resistive switching are illustrated in Figure 4.

In a unipolar mode (Figure 4A), the change in the resistance state only depends on the magnitude of applied voltage and not the polarity. The Set process (toward On state) is always established at higher voltage than that required for the Reset operation. The level of current reached at the Reset transition point is also greater than the compliance defined during the Set operation. In a bipolar mode (Figure 4B), the use of opposite voltage polarities is a key requirement to switch the devices On (Set) and Off (Reset), respectively. Frequent asymmetry of the I-V curve characteristic is also observed with both switching modes and can be tailored through device fabrication or electrical forming [1].

Although the resistance switching is electrically induced in both modes, the concrete driving force is quite different, depending on the relative implication of the electric field and Joule heating on controlling the formation and stability of conductive channels. Generally speaking, a memristive switching tends to be unipolar when Joule heating effect dominates and bipolar when electric field effect is mainly involved [1].

3.1 Unipolar switching behavior

A plausible explanation for unipolar switching of metal oxide memristors is a fuse-antifuse mechanism relying on a filamentary model with the Joule heating effect as a key driving force for mass transfer. According to this view, the Set and Reset transitions are achieved, respectively via the thermally-induced formation and rupture of nano-width conductive filaments stretching over the entire oxide layer.

For instance, the formation of conductive filaments in unipolar anionic switches (i.e. Pt/TiO$_2$/Pt/Au) is attributed to a steep gradient of inner device temperature at the threshold Set or forming voltage, leading to thermophoresis and/or oxygen ion diffusion within the insulator region [13]. A thermal mapping investigation of the Reset transition of unipolar Pt/NiO/Pt anionic devices suggests that filament rupture occurs by heat-induced solid phase dissolution of oxygen species at very high current densities (strictly beyond the initially set compliance current) [12, 36].

Unipolar resistive switching is rarely observed with cationic devices, since the heat-induced migration mechanism is not yet fully developed within the ECM theory. General observations only imply the dependence of the R_{On} resistance range of unipolar devices on the conductivity of the insulator layer before thermal breakdown.
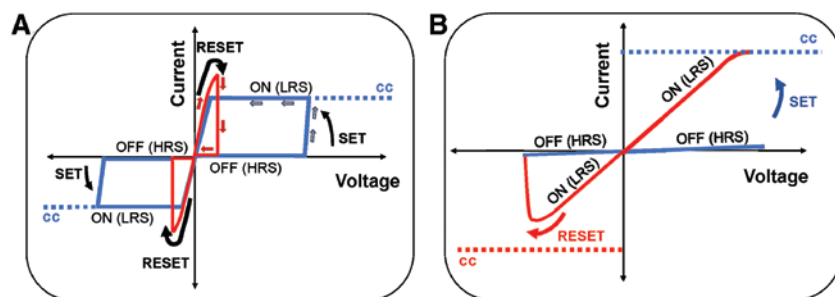
Figure 4: Schematics of I-V curve switching characteristics of memristors. (A) unipolar mode; (B) bipolar mode. cc, compliance current.

Only few examples of temperature-dependent switching studies of unipolar cationic systems (i.e. $Cu/Ta_2O_5/Pt$ and Cu/Cu-doped-ZrO_2/Pt) suggest an assistant thermal-diffusion path of metallic species that contributes to the Reset event [37, 38]. Furthermore, the geometry of conductive filaments and their growth dynamics remains disputed. For example, a recent in situ electronic imaging of devices under programming suggested that cationic conducting channels may be composed of nano-island structures rather than co-continuous filaments [39, 40]. Hence, further experimental studies are necessary to clarify the directionality of metallic migration in cationic devices and the level of implication of the inert or active electrode interface on inducing and defining the dynamics of filament rupture in the Reset process.

3.2 Bipolar switching behavior

Bipolar resistive switching is observed in most metal oxide cationic devices and in similar anionic systems. It is often associated with a nano-ionic transport mechanism that is governed by redox equilibria and is mainly driven by an external field.

The classic polarity dependence fingerprint of a bipolar switching regime of cationic switches is reasonably explained by the ECM theory. The formation of conductive channels during the Set transition requires a positive bias on the AE to release cations, which will be reduced into metallic filaments at the (inert) counter electrode surface. Reversing the polarity triggers the Reset event via backward oxidative dissolution of the metallic filaments, which induces the progressive destruction of the electrodes' connectivity with existing conductive channels spanning the bulk solid electrolyte [11]. The dynamics of filament growth in cationic metal oxide devices showing a bipolar switching regime are rarely explored in the literature [7]. An example model is depicted in cationic devices (ECM) having a different insulator system when compared

to metal oxides, such as in the case of Ag/Ag-GeSe/Pt electrochemical cell [41]. According to this model, metal filaments grow in a preferential direction of the active electrode (Ag) during the Set process (i.e. in a direction opposite to the migration of cations). Once the metallic filaments reach the active electrode surface, they create a galvanic metallic contact between the two electrodes, which allows the device to switch On. If a sufficient voltage of opposite polarity is applied, electrochemical dissolution of metal filaments will take place to Reset the device to its initial Off state.

Generally speaking, the switching speed of bipolar cationic devices (bipolar ECM) is mainly determined by the kinetics of the various electrochemical processes involved in the formation and rupture of conductive metallic filaments.

The underlying mechanism of bipolar switching in anionic systems is better explored in literature in regard to oxygen anion motion (VCM). A main interpretation of this phenomenon is that the viable resistance state of an anionic device depends on the oxygen affinity of the electrode metal and the height of the Schottky barrier formed at the electrode-active insulator junction [42, 43]. An important question concerns the typical electrode polarization in the Set and Reset processes. For a p-type semiconductor oxide (where holes are the majority charge carriers), few mobile oxygen ions exist near crystal defects involving grain boundaries (i.e. dislocations). When a positive voltage is applied to a terminal electrode having a high affinity towards oxygen species, mobile oxygen anions migrate (via drift or electro-migration) towards it and progressively accumulate in its proximity. The resulting abundant negative charge helps narrow the depletion region at the electrode interface, leading to a stable reduction of the electron potential energy barrier (or Schottky barrier height). When the interfacial depletion width is sufficiently narrowed down, assistive electron tunneling further minimizes the contact resistance until the device is switched On (HRS to LRS). For the Reset process, a

negative bias is applied to the same terminal electrode, to create an opposite phenomenon via electrostatic repulsion, which forces the accumulated oxygen anions to move away from the electrode surface. An ion-transport recombination model is proposed by Gao et al. [44] to explain the migration of oxygen ion species back into the insulator bulk. According to this model, oxygen ions move away from the negatively polarized electrode and recombine with bulk oxygen vacancies through which conductive filaments eventually get destroyed, leading to a reset switching event (i.e. from LRS to HRS).

In regard to the dynamics of bipolar switching in anionic devices, linear (i.e. super-exponential) and nonlinear I-V bipolar loops are generally recognized, depending on the implication level of the electric field into the kinetics of the ion-transport mechanism and into the observed current (in addition to dissipated power and heat) [45–49]. Practically, there is no sharp switching threshold voltage defined for memristive devices, due to their large dependence on the smallest variability of memristor chemistry, mainly stemming out of the different fabrication processes explored. It is important to mention that nonlinearity in ionic transport behavior is substantial for simultaneously achieving fast switching speeds and long retention times in memristive devices [50–53].

3.3 Mixed bipolar/unipolar switching behavior

Several metal oxide systems including those based on transition metal elements show atypical co-existent bipolar and unipolar resistive switching. Examples of these oxides include TiO_x [16, 54], ZrO_x [55, 56], MoO_x [57], AlO_x [58, 59], and HfO_2 [60, 61]. In these devices the external current is the crucial factor determining whether the device will be in a bipolar switching regime (usually at low current) or in a unipolar mode (usually at high current due to Joule heating). The main reason for this mixed behavior is yet unclear but can possibly be explained in terms of formation and rupturing of conductive filaments. At low currents, it is difficult to generate an optimal temperature that allows the rupture of conductive filaments, whereas by applying small current it may be possible to drift the oxygen vacancy towards the formation of conductive filaments. A compliance current dependency is particularly believed to affect the switching regime in some of those devices. An example study carried on TiO_2 thin films describes a resistive bipolar switching regime at low current range and unipolar switching characteristics at a greater value of compliance current [54].

4 Effect of electrodes

The impact of the electrode material on the resistive switching of memristive devices is extensively reported as one of the crucial factors in device fabrication, due to potential chemical interplay existing at the contact surface with the active material [62–64]. For example, cation interdiffusion, lack of phase stability, and interfacial reactions involving vacancy migration from the electrode surface towards the insulating layer should be critically examined during the electrode selection process. Typical side interactions usually dictate how the device will behave after a prolonged period of operation and are primarily dependent on the electrode work function (i.e. electron removal ionization energy), in addition to structural similarities with the insulating layer sub-lattice (i.e. elemental size and crystal phase) [52–55].

It is important to mention that the work function criterion must be carefully interpreted since it is usually highly sensitive towards crystal orientation and hence the ways of measurements for the pure electrode material. The effective work function is also completely altered by the nearby composition of the contact surface, which mainly evolves from the electrode deposition process and from interfacing inside the sandwiched MIM structure [65–67].

Figure 5 summarizes the absolute work function of a wide variety of native metals and semiconductor materials including those considered in memristor electrode stacks such as aluminum (Al), titanium (Ti), copper (Cu), nickel (Ni), noble metals like platinum (Pt), gold (Au), and ruthenium (Ru), and metal nitrides (TiN, AlN) [68, 69]. A low work function and high oxygen affinity of the electrode material is sometimes regarded as substantial for reducing the forming voltage. For instance, Cagli et al. [70] concluded that a Ti electrode, which is considered as a strong oxygen getter (acceptor), effectively reduces the forming voltage of HfO_2 memristors by sourcing out interfacial oxygen atoms leading to sub-stoichiometric HfO_x regions within the bulk switching film. Nevertheless, it is widely accepted that high work function elements can easily block ion transport and would be more suited for electrode materials to minimize side interactions that may cause irreversible changes within the memristor switching mechanism, ultimately impacting the device's endurance.

The impact of electrode nature on resistive switching has also been of extensive research for the late development of advanced atomic and molecular-scale electronics [63, 70]. In MIM two-terminal devices, the resistive switching is mainly observed when a positive voltage is applied to the top electrode resulting into higher-resistance state programming [71]. The location where each filament
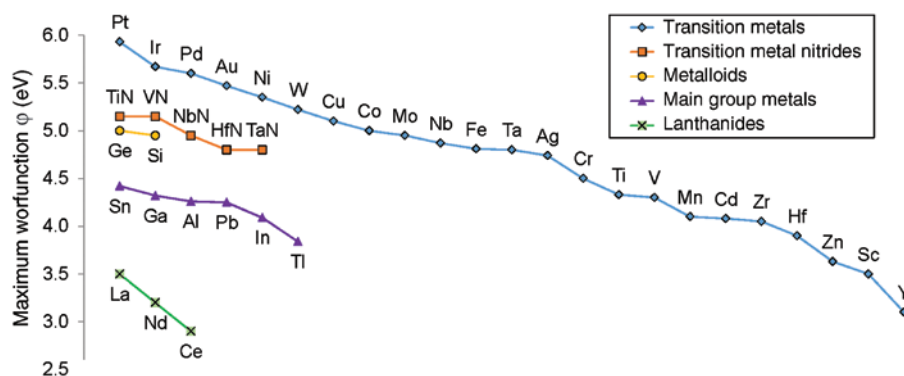
Figure 5: Native work function of various metal and semiconductor elements [68].

ruptures during the Reset operation seems to largely depend on the type of electrode material. For example, Cagli et al. [70] demonstrated that having top and bottom Pt electrodes leads to unipolar switching in HfO_2 memristors, whereas mixed TiN-Pt or TiN-Ti electrode systems result in bipolar characteristics. The origin of filament rupture is not well established particularly for ECM (or cationic) devices. Example studies on HfO_2 devices with Ti, TiN, or TiON top electrodes and Pt or Ru bottom electrodes showed that filament rupture occurs near the top electrode interface [72–75], while other studies supported the implication of the bottom electrode at inducing the Reset process [71, 76, 77].

An example of real-time dynamic observation of conduction channels in $Ag/ZrO_2/Pt$ cationic system reveals the initiation of filament rupture at the interface between the conduction channel and the inert counter electrode Pt (acting as anode) [78]. More research is still needed to elucidate the fundamental nature of the switching regime of cationic devices from the microscopic point of view.

For ZnO memristive devices, the effect of metal electrodes on memristor switching behavior is explained in terms of differences observed on the active and electrode materials work function. Recently, Kumar and Baghini [79] demonstrated that a high work function electrode such as Pt can yield a more pronounced hysteresis curve compared to Cr, owing to larger difference between the Pt and ZnO work function. This observation was interpreted with the ability of a Pt/ZnO interface to form a Schottky contact and a depletion layer, which varies with applied external voltage, as opposed to non-switchable Cr/ZnO system [79]. However, when the Pt electrode was replaced with a similar work function material such as Au, a narrower hysteresis curve was recorded. In this case, the soft material properties of Au promote its diffusion into the ZnO interface, which results in the modification of the Schottky contact

via the creation of Zn vacancies and the subsequent reduction of the R_{Off}/R_{On} ratio of the device [79].

The area of the electrode contact is a frequently neglected synthetic parameter and could be an important target for further device optimization. The possible implication of the electrode area is assumed on distinguishing two different geometrical localizations of the switching event: (i) the single filament model and (ii) the area-distributed switching [11, 80]. Typical switching scenarios can be differentiated by measuring the area dependence of the low-resistance state. The On resistance would be completely independent of the electrode area when the Set event only requires the formation of a single filament [80–82]. In this case, the remaining non-switching electrode area would be contributing to a parallel resistance, and the nanoscale size of the filament should hence be considered to determine the ultimate scaling limit of the device [18, 83]. When the switching occurs more or less homogeneously over the entire active layer, the On resistance is found to increase almost proportionally with the electrode area [84, 85]. Hence, scaling down should be considered to improve the R_{Off}/R_{On} resistance ratio.

In summary, the electrode material properties like work function, oxygen affinity, and softness significantly affect the switching mechanism and the subsequent I-V dynamics of memristive devices. It is critically important to further understand the effect of the electrode material on other salient features of device operation, including retention time, endurance, Set and Reset voltages, and R_{Off}/R_{On} ratios.

5 Effect of capping layer

The capping is often regarded as a thin buffer layer that can be placed between the top or bottom electrode and

the active insulator matrix to improve the switching properties of the memristor devices (i.e. retention time, resistance range, and switching speed). The use of a capping layer is mostly reported with anionic devices where it essentially serves on enhancing the switching dynamics by promoting the diffusivity of oxygen species or vacancy carriers. Examples of capping materials include low-resistance metal oxides (i.e. ITO) [86] or metals of similar or different nature than that present in the insulator matrix (i.e. Ti, Zr, Al, and AlCu) [64, 71, 87–91]. The affinity of the capping material towards oxygen anions particularly dictates the extent of vacancy migration and hence the speed at which conductive filaments are formed [90, 92]. For instance, it has been reported that a Ti over-layer is more adequate for capping interposed metal oxide – high-k dielectric stacks – than Al, owing to its higher oxygen-scavenging properties [93].

Studies on $TiN/HfO_2/TiN$ memristor reveal that the introduction of a thin Ti buffer layer into the MIM structure induces the formation of a TiO_X/HfO_X bi-layer, which increases the resistance range and improves the overall switching speed and endurance of the device when compared to the performance of a native switching material [87, 91].

The type of capping layer material also affects the HRS/LRS current ratios and the operation voltage window, in view of distinctive kinetics introduced on oxygen and vacancy-related trap formation and destruction. For $TaN/$(capping)$/HfO_2/Pt$ memristive device structure, studies show that Zr capping results into lower V_{SET}/V_{RESET} values, larger window between LRS and HRS current, and better HRS current stability at high temperatures (up to 110°C) than Ti capping [88].

Besides the oxygen affinity of capping layer, another important factor to consider is the bonding energy between the capping material and oxygen. Wang et al. [94] used a thermodynamic quantity, which is the molar Gibbs energy, to quantify the bonding between the capping material and oxygen atoms migrating from the active layer. The study concluded that capping materials with high molar Gibbs energy can hold oxygen atoms so tightly that it becomes difficult to rupture local conducting filaments during the Reset operation.

6 Insulating-layer materials in MIM memristors and fabrication processes

The selection of an appropriate active material is another crucial step in memristor device fabrication. A variety of factors including mainly the semiconducting properties and the inevitably associated Joule heating effects are decisive in the design of operational MIM stacking [95]. For the device to have resistive switching characteristics, it requires an active layer with dual conductive and insulating behavior [1]. Established manners that ensure the formation and rupture of conductive filaments in semiconducting metal oxide systems are (i) the usage of ready-made non-stoichiometric active materials [96–99], (ii) doping the insulator with one or more metal or metal oxide [100, 101], and (iii) interfacing the insulator with a buffering agent layer [61, 87, 89, 102, 103], as illustrated in Figure 6.
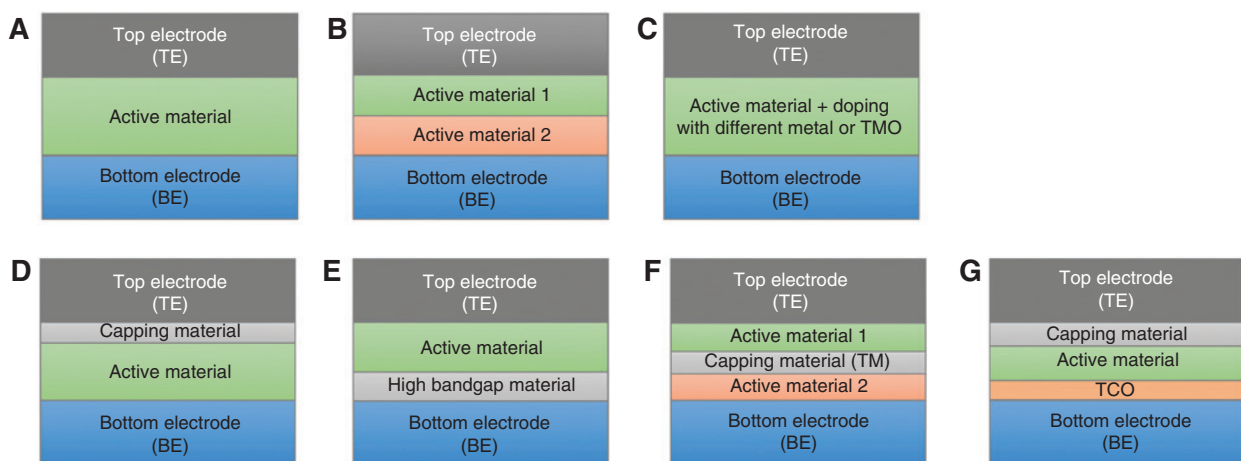
Figure 6: Examples of MIM stacks considered in metal oxide memristor literature. (The relative sizes of the layers are for illustration purposes only.) (A) [96, 97]; (B) [98, 99]; (C) [100, 101]; (D) [61, 87, 89]; (E) [102]; (F) [103]; (G) [86].

Table 1: Examples of bipolar metal oxide memristors and their operational characteristics.

Material	TE/BE	V_{SET}/V_{RESET}	$\Delta R = R_{Off}/R_{On}$	Switching speed	Retention time	Endurance	Fabrication process	References
ZnO	Ag/Cu	1.2 V/-1.25 V	1000	–	–	>500 cycles	Electrohydrodynamic printing	[110]
TiO$_2$	Pt/Pt	1 V/-0.5 V	100	10 ms	–	10^6 cycles	RF-magnetron sputtering	[111]
	Pt/Pt	–	100	–	–	–	ALD	[112]
	TiN/Pt	+1 V/-1.5 V	10	1 µs	10^4 s	10^4 cycles	RF-reactive sputtering	[97]
	TaN-TiN/TiN-TaN	1.5 V/-1.5 V	1.5	–	–	10^2–10^3 cycles	Sputtering	[113]
LaO	Al/Al	3 V/-2 V	~50	–	10^4 s	100 cycles	Plasma-enhanced ALD	[114]
	ITO/SrTiO$_3$	5 V/-1.6 V	200	–	>4×10^4 s	2000 cycles	Pulsed laser deposition	[115]
TaO$_x$	Pt/Pt	–	–	–	10 years at 85°C	10^9 cycles	Sputtering	[116]
	W/Pt	–	–	–	>10 years	10^4 cycles	RF-magnetron sputtering	[117]
NiO	Pt/Pt	>10 V/<-10 V	–	–	>10^4 s	–	Pulsed laser deposition	[118]
	Au/Au	+5.2 V/-6 V	–	–	–	–	Electrochemical plating	[96]
HfO$_2$	TiN/TiN	1.5 V/-1.4 V	100	<10 ns	>500 min at 200°C	>10^6 cycles	ALD	[93]
	TiN/TiN	–	>50	5 ns	10^5 s at 200°C	5×10^7 cycles	ALD	[61]
ZrO$_2$	ITO/Ag	1 V/-1 V	>10	–	10^6 s at 27°C	>50 cycles	Electrohydrodynamic printing	[119]
	Ag/Ag	3 V/-3 V	~100	–	–	–	Electrohydrodynamic printing	[120]
	TiN/Pt	0.8 V/-0.5 V	–	–	10^4 s at 27°C	10^3 cycles	RF-magnetron sputtering	[121]
CeO$_2$	Au/Au	2.4 V/-3 V	10^4	–	–	–	Sol-gel (drop-coating)	[122]
AlO$_x$	Al or CNT/CNT	–	–	–	–	10^4 cycles	ALD	[123]
	Cu/W	1.3 V/-0.05 V	500	–	10^5 s	–	E-beam evaporation	[124]
Al$_2$O$_3$	Ti/Pt	1.4 V/-1.7 V	<1000	10 ns	10^3 s	–	RF-magnetron sputtering	[59]
Cu$_2$O/CuO	Pt//Nb-STO	–	10^5	–	10^4 s	–	Plasma assisted molecular beam epitaxy	[125]
Gd$_2$O$_3$	ITO/ITO	+2 V/-2 V	–	–	–	10^3 cycles	Pulsed laser deposition	[126]
GdO$_x$	Cr/TiN	<+4 V/-4 V	>70	–	3×10^4 s	10^5 cycles	E-beam evaporation	[127]
MnO	Ti/Pt	0.7 V/-1.1 V	–	–	10^4 s at 85°C	10^5 cycles	RF-reactive sputtering	[128]

TE, top electrode; BE, bottom electrode; "–", data not found in the associated reference paper.

Table 2: Examples of bipolar mixed metal oxide memristors and their operational characteristics.

Material	TE/BE	V_{SET}/V_{RESET}	$\Delta R = R_{Off}/R_{On}$	Switching speed	Retention time	Endurance	Fabrication process	References
Cu doped SiO$_2$ bipolar-unipolar	Cu/W	0.9 V/-0.75 V	$10^3/10^6$	–	5×10^4 s	10^7 cycles	E-beam evaporation	[129]
Cu doped ZrO$_2$ bipolar-unipolar	Au-Cu/Pt-Ti	3.6 V/-1.5 V	10^6	50 ns (Reset→Set) 100 ns (Set→Reset)	10^4 s	–	Thermal evaporation	[100]
ZnO$_{1-x}$/ZnO bilayer structure	Pt/Pt	1.5 V/-0.6 V	40	–	>10^4 s	100 cycles	Sol-gel	[130]
ZnO/NiO	Au/n-Si	8 V/-8 V	–	–	–	–	Ultrasonic spray pyrolysis	[98]
ZnO/ZnWO$_x$ bilayer structure	Pt/W	0.8 V/-0.6 V	300	–	–	>200 cycles	Sputtering	[131]
ZTO	Al/Pt	0.25 V/-0.85 V	>1000	–	>10^4 s	>50 cycles	Sol-gel (spin coating)	[132]
TiO$_2$/Cu$_x$O	Ti/Cu	2.5 V/-1V	–	50 ns	up to 30 h	–	Electrochemical deposition	[133]
HfLaO$_x$	TaN/Pt	2.27 V/-1.81 V	10^6	10 ns	10^4 s at 27°C	10^4 cycles	ALD	[134]
MgO/CoO$_x$	Pt/Au	15 V/-3 V	12.5	–	>10^2 s	10^8 cycles	Pulsed laser deposition	[135]
WSIOx	Pt/TiN	2 V/-2 V	–	–	10^5 s at 250°C	10^5 cycles	RF-magnetron sputtering	[136]
WSIOx/WSiON	Pt/TiN	–	<10^5 at 85°C	–	–	10^8 cycles	RF-magnetron sputtering	[137]
Pt-dispersed SiO$_2$	Pt/Ta	–	–	<100 ps	>6 months	>3×10^7 cycles	RF-magnetron sputtering	[138]
Au doped HfO$_2$	Cu/Pt	0.34 V/-0.9 V	10^2	–	–	–	RF-reactive sputtering	[139]
TiO$_x$/HfO$_2$	TiN/TiN	1.5 V/-1.4 V	>1000	5 ns	10 years at 200°C	>10^6 cycles	ALD	[93]
AlHfO$_2$/Cu	Cu/n+Si	4 V/-6 V	10^3	–	10^4 s	–	RF-magnetron sputtering	[140]
AlCu/HfO$_2$	TiN/TiN	<1V/>-1V	–	<50 ns	3×10^4 at 85°C	10^5 cycles	ALD	[89]
AlO$_x$/TaO$_x$	W/TiN	–	–	–	>10 years at 85°C	10^6 cycles	E-beam evaporation	[141]
AlO$_x$/WO$_x$	Al/W	1.4 V/-0.8 V	–	–	10^4 s	–	Rapid thermal oxidation (RTO)	[99]
Nitrogen doped WOx	Ti/Pt	2 V/-2 V	–	–	10^4 s	>10^2 cycles	RF-reactive sputtering	[101]

TE, top electrode; BE, bottom electrode; ZTO, zinc tin oxide; "—", data not found in the associated reference paper.

Table 3: Examples of unipolar metal oxide memristors and their operational characteristics.

Material	TE/BE	V_{SET}/V_{RESET}	$\Delta R=R_{Off}/R_{On}$	Switching speed	Retention time	Endurance	Fabrication process	References
CoO_x	Pt/Pt	–	–	–	10^4 s	10^3 cycles	RF-sputtering	[142]
Co_3O_4	Pt/Pt	1.9 V/-0.52 V	5×10^3	–	–	–	Cold pressing	[143]
CuO_x	Al/Cu	–/0.7 V	–	–	–	10^4 cycles	Electrochemical plating	[144, 145]
Gd_2O_3	Ti/Pt	2.5 V/1.2 V	–	–	–	10^2 cycles	Pulsed laser deposition	[146]
NiO	Nobel Metals	–	–	–	2×10^7 s	10^{12} cycles	RF-sputtering or plasma oxidation	[147]
SnO_2	Pt, Au,Tl/Pt	1.5–2 V/0.5–1 V	–	–	10^4 s	10^2 cycles	Pulsed laser deposition	[148]
HfO_2	Ni/TiN	–	–	–	–	10^2 cycles	ALD	[63]
WOx	TiN/W	–	–	>50 ns	10^4 s at 100°C	10^7 cycles	Rapid thermal oxidation	[149]
Ti-embedded ZrO_2	Ti/Pt	-1.2 V/-0.7 V	–	–	10^5 s	10^3 cycles	RF-sputtering	[150]

TE, top electrode; BE, bottom electrode; "–", data not found in the associated reference paper.

Active materials are generally categorized based on their anionic composition (i.e. oxides, tellurides, sulfides, and nitrides [22]), crystal structure (i.e. amorphous and perovskites [1]), and dimensionality (i.e. zero, one, and two with respect to nanoparticles [104] nanowires [105], and films [106]) but more prominently according to their unipolar and bipolar switching behavior [22, 107, 108]. Our particular focus on metal-oxide-based insulators is in view of their simplistic atomic structure, good thermal stability, compatibility with mature CMOS processing, and optimum switching characteristics [107, 109]. Tables 1–3 provide a mapping of important operational memristive characteristics of various physical MIM metal oxide systems reported in the literature. The devices are listed according to their bipolar/unipolar switching nature and according to their chemical composition [59–61, 87, 89, 91, 96–101, 110–150]. Examples of relevant electrical performance descriptors include V_{SET} and V_{RESET} (or voltage sweep window), R_{Off}/R_{On} ratio, switching speed, retention time, and endurance. Of the quantitative data collected, a large variability is generally observed on the electrical performance characteristics and behavior of metal oxide memristor devices, due to non-standardized testing conditions and high intrinsic implications of (i) historical processing operations, (ii) stack configurations and elementary compositions, and (iii) elaboration methods. For example, the fabrication of an active insulator layer can be performed via various techniques (Tables 1–3), which are generally based on (i) physical deposition, such as sputtering [3, 9–11, 19, 43, 113], electron beam evaporation [124, 129], pulsed-laser deposition [115], thermal evaporation [100], and electro-hydrodynamic printing [119, 120] or on (ii) chemical transformation such as atomic layer deposition (ALD) [16, 95, 112], ultrasonic spray pyrolysis [98], rapid thermal oxidation [101], plasma-enhanced

molecular beam epitaxy [125], and sol-gel process [122, 151, 152]. Particularly, radio frequency (RF) sputtering is considered as the most popular approach for large area-uniform thin-film deposition, owing to its high yield with nano-metric thickness control capabilities and low cost of operation [107]. For advanced nanoscale fabrication, greater focus is made on ALD process, which further allows a chemically uniform deposition at one-atomic-scale resolution. The ALD route also allows for selective tuning of the material composition via the introduction of chemical dopants [153] and control of oxygen vacancy concentration [17]. Finally, the sol-gel process is regarded as the least expensive approach but is mainly useful for microscale engineering [152]. In conclusion, the growth temperature will be the decisive factor in determining the CMOS processing compatibility of metal oxide memristor devices. Any fabrication process anticipated of the above will certainly have a different implication on the thermo-mechanical stability and ion migration properties, which should be mapped against the cost of durability, scalability, and performance reproducibility of the devices.

7 Prospective applications

Application areas of memristor devices, as illustrated in Figure 7, are numerous owing to their versatile nature in terms of elementary design structure and their CMOS fabrication compatibility along with their superior operational characteristics in terms of switching speed, retention rate, and endurance. One of the promising uses of memristor devices is "non-volatile memory" for computing. Table 4 summarizes some of the key parameters of existing commercial memory technologies and emerging ones [154]. As can be seen from the table, a memristor has the density

Table 4: Key specifications of state-of-the-art commercial memory technologies vs. transpiring memristor device.

	Available commercial technologies				Transpiring technology
	DRAM	**Flash (NAND)**	**Flash (NOR)**	**SRAM**	**Memristor**
Cell density (F^2)	6–30	1–4	1–10	140	4
Retention time	>64 ms	>10 years	>10 years	as long as voltage is applied	>10 years
Endurance	>10^{16} cycles	>10^5 cycles	10^5 cycles	>10^{16} cycles	>10^{12} cycles
Read time	2 ns	0.1 ms	15 ns	0.1–0.3 ns	<2 ns
Feature size	36 nm	16 nm	45 nm	45 nm	<5 nm
Device cell element	ITIC	1 T	1 T	6 T	1 R/1 T 1 R
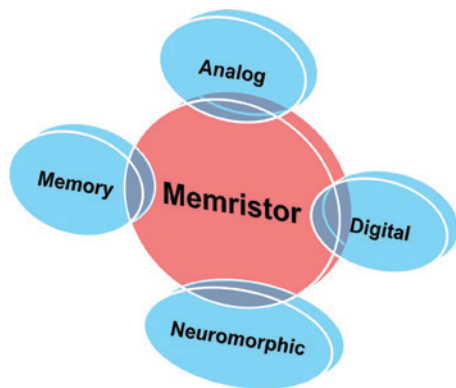
Figure 7: Potential pillar applications of memristor devices.

of the dynamic random-access memory (DRAM) and the speed of the static random-access memory (SRAM), which makes it ideal for universal and Content Addressable Memory-type (CAM) memory [155]. The non-volatile nature of memristor also enables the zero-leakage power for memory and can be used as part of the power management unit in wireless sensor nodes [156, 157]. Memristor devices can also be used for analog applications including programmable analog circuits, analog filters, oscillators, and chaotic analog circuits [158, 159]. In particular, the introduction of memristor technology could help increase the linear range of analog amplifier circuits as opposed to traditional setups [155, 156, 160]. Memristor devices also have potential uses in digital logic applications supporting in-memory computing [161, 162]. While analog systems are constructed with memristors having continuous resistance change, digital applications require stable discrete resistance state [107]. One of the most promising digital applications of memristor devices is as field-programmable gate array (FPGA) [163]. A discrete FPGA architecture was reported by Cong et al. [164] where interconnections are designed only by memristors and show a reduction of up to 5.5 times and 1.6 times, respectively, on achievable device area and power requirement. Current developments are also being projected towards neuromorphic

applications to span the cognitive computing [165–167]. In a typical area, the memristor would be implemented as an electronic synapse, where it could mimic the electrical response of the elementary structures in the human brain, allowing for replacement of defective neurons. Until now, several non-volatile technologies have been tested as electronic synapse, such as resistive random-access memory (RRAM), ferroelectric tunneling junctions, and magnetic tunnel junctions [165]. To date, RRAM is the most reliable technology owing to its famous operation characteristics.

8 Conclusions

Memristor devices have a high potential in replacing some of the current technologies used for nonvolatile memory. However, there are still momentous challenges to overcome before this happens. Decisive factors are the integration and reliability of the device, which are substantial for industrial manufacturing. Device implementation currently waits for robust material processing and uniformity of engineered interfaces, since the device characteristics, such as retention, endurance, and switching speed are immensely affected by the fabrication process. The reliability of the memristor device also needs to be taken into consideration before it can be used at a large scale. Testing the device and characterizing its failure modes with respect to temperature and read and write cycles are so important from a quality control point of view. Another imposed challenge is to have in-depth understanding of the switching mechanism, which will allow for further structural and performance optimization of the device. Developing robust device models that truly reflect the operation of memristors and integrate them with electronic design automation tools is another major challenge. The described challenges have focused the attention of researchers across the various domains related to memristor, which span device fabrication through applications. The intensive research effort over the past few years, in

particular, has resulted in many promising solutions that are shaping memristors into a viable future technology.

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