Research article

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On-chip optical spatial-domain integrator based on Fourier optics and metasurface

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Abstract: Analog optical computing has been an innovation and research interest in last several years, thanks to the ultra-high speed (potential for real-time processing), ultra-low power consumption and capability of parallel processing. Although great efforts have been made recently, no on-chip optical spatial-domain integrator has been experimentally demonstrated, to the best of our knowledge. Based on Fourier optics and metasurface, we design and fabricate an on-chip optical integrator using silicon-on-insulator (SOI) platform. The proposed integrator is able to integrate the electric field in spatial domain. As a proof-of-concept demonstration, a representative optical signal is well integrated to the desired distribution. Compared with theoretical expectation, the similarity coefficients of the simulated and experimental results are 83 and 78%, respectively. The proposed scheme has potential of performing more complex and ultra-high-speed computing for artificial intelligence.

Keywords: Fourier transformation; metasurface; optical computing.

1 Introduction

Recently, unprecedentedly large computing power is urgently needed, while developing advanced process for traditional electronic signal processing is becoming much more difficult and expensive. Consequently, various new computing platforms have been proposed, such as biocomputing [1], quantum computing [2], neuromorphic computing [3] and optical computing [4]. Having obvious advantages of ultra-high speed, ultra-low power consumption and parallel-computing capability, optical computing is placed high hopes for prospective ultra-high-speed computing.

Limited by bulky devices and difficulty of regulation, the general-purpose digital optical computing [5] remains an intriguing concept, while analog optical computing (AOC) dedicated to a single purpose develops rapidly with the leap forward of artificial intelligence. Since the idea of performing spatial AOC with metamaterials was first proposed by Silva et al. [4], a few spatial-domain devices have been illustrated, such as spatial filter [6], differentiator [7–11], integrator [9, 11–13], convolver [14], equation solver [15, 16] and correlator [17, 18]. Being different from time-domain devices [19, 20], signals in these devices are distributed in spatial domain and the computing is performed by realizing the desired transfer function with spatial Fourier transfer approach or Green's function approach. As a novel structure that can freely regulate light field as desired and has the advantages of being compact, the metasurface seems a perfect candidate for AOC [21, 22]. However, most metasurface-based optical computing systems are established in free space, and assembling those free-space systems remains a tough task. Therefore, the chip-scale integrated AOC system is quite attractive, and previous researches have illustrated the on-chip AOC devices [7, 11, 14, 15, 23]. Unfortunately, no experimental demonstration of on-chip optical spatial-domain integrator has been investigated, to the best of our knowledge.

Here, a novel symmetry-slot on-chip metasurface is proposed to perform optical spatial-domain integration based on Fourier optics. By engineering the width and length of each slot using the silicon-on-insulator (SOI) platform, the fully control over the transmitted intensity and phase profile can be achieved. Two identical metalenses are utilized to perform the Fourier transforms in a 4-*F* system [24, 25], and the specially designed metasurface is embedded in the middle to carry out the integral

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operation at the Fourier plane. The whole device has a compact footprint, with length and width of 67 and 14 μm, respectively. In a proof-of-concept demonstration, the output distribution fits well with desired curve under the incidence of a representative light field at 1550 nm with transverse electric (TE) mode. By comparing with theoretical results, similarity coefficients of 83 and 78% are obtained for simulation and experiment, respectively, proving the feasibility of the proposed scheme. Furthermore, the simulation under different incidences clarifies the universality of the proposed integrator.

2 Operation principle and device design

As shown in Figure 1, the input signal $f(y)$ is incident at the input plane of a 4-F system that composed of three specially designed metasurfaces, i.e. two identical metalenses and a middle metasurface (MMS). With the first metalens performing Fourier transform to the input signal, the distribution of spatial frequency is presented at the Fourier plane, where the MMS is settled for manipulation. The manipulated light pattern is then converted back to spatial domain with the assistance of the second metalens. According to the integral properties of spatial Fourier transformation, the ideal complex amplitude transmittance function of the MMS is assigned to be $T(y) = \lambda f/(jy)$. It should be noticed that the function has to be handled in the actual design as follows near the singularity at $y = 0$:

$$T'(y) = \begin{cases} T_m, & |y| < d \\ T_m \cdot \dfrac{d}{y}, & |y| \geq d \end{cases} \tag{1}$$

where T_m is an appropriate constant and d is relatively short compared with the length of transverse modulation range at Fourier plane [4, 26]. The inset in Figure 1 presents the amplitude transmittance and phase-shift function of the MMS indicated by Equation (1). As for the metalenses, the transmission characteristics are only related to a space-dependent phase shift:

$$\phi(y) = -\frac{\pi y^2 n_{\text{eff}}}{\lambda f} \tag{2}$$

where λ, n_{eff} and f represent the wavelength of input signal, effective refractive index and focal length of the metalens, respectively.

To realize the proposed scheme in an easy-to-fabricated way, a symmetry-slot metasurface is designed to manipulate the light field as required by Equations (1) and (2). Schematic diagram of the proposed metasurface is shown in Figure 2(A), with input light traveling along the x-axis. For each unit of the metasurface, a slot is etched off on the Si layer with thickness of $h = 220$ nm. Different units with specific footprints are lined along y-axis to construct the metasurface, while the center spacing of the adjacent units is $\Lambda = 500$ nm. By elaborately designing the width and length of each slot, the amplitude and phase shift of incident light can be properly manipulated, from $f_{\text{in}}(y)$ to $f_{\text{out}}(y)$, as desired.

The structure is designed and simulated using the finite difference time domain method. The refractive indices of Si and SiO_2 are 3.48 and 1.44 at 1550 nm, respectively. Figure 2(B) and (C) shows the simulated results under incidence of a quasi-plane wave on-chip (whose wavefront is flat in the y direction, as can be seen in Figure 2(C)) for different slot designs. As marked with black rectangles in the figures, the slot width/length combinations are 0.1/3.0, 0.2/0.1, 0.3/1.1 and 0.4/2.0 μm, respectively, from top to bottom. It is inspired that the

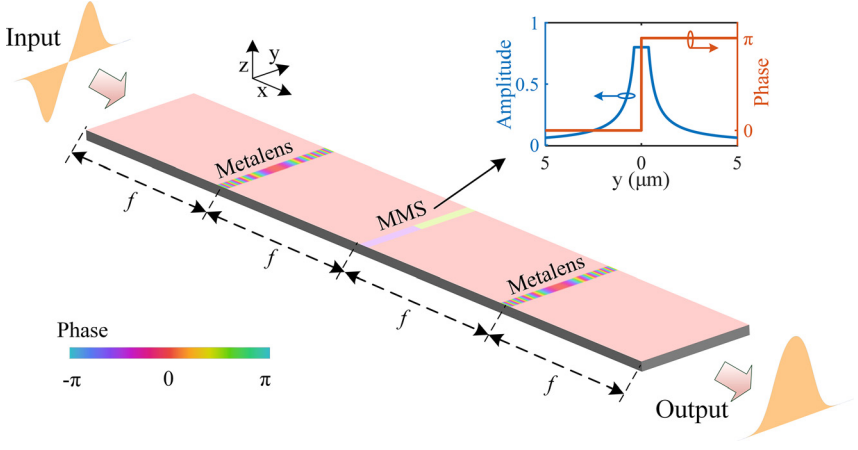

Figure 1: Schematic diagram of the proposed integrator. The color of the three metasurfaces in the diagram represents the phase characteristics.

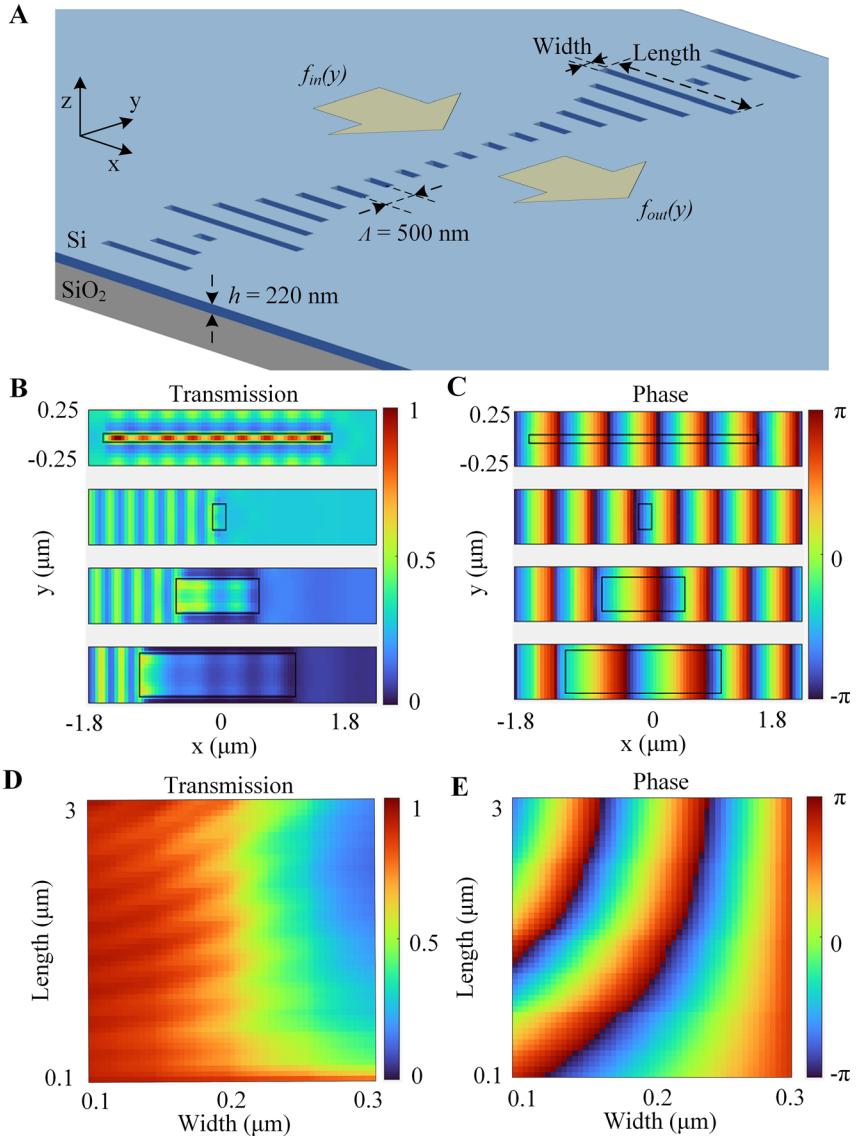

Figure 2: Framework and properties of the metasurface.
(A) Perspective view of the designed framework. (B and C) Unit simulation under different slot width/length combinations. (D and E) The attained modulation library.

output profile of both intensity and phase are visually flat, indicating that the slot affects the output light distribution uniformly. On account of the fabrication requirement, the width and the slot spacing are limited to 140 nm while the longest length is set to 3000 nm. The corresponding regulation of the intensity and phase shift are presented in Figure 2(D) and (E) individually, providing a modulation library for actual design. The intensity modulation ranges from 0.13 to 0.94, and the phase shift range is as large as 16.94 rad, indicating that the modulation range fulfills our requirement. Based on the attained modulation library, the proposed optical integrator can be comprehensively designed as follows.

Firstly, two metalenses are introduced for spatial Fourier transform in a 4-*F* system. To be noted, the intensity modulation is mainly determined by the width of the slot and the transmission of light intensity increases with the width decreasing (Figure 2(D)). For highest transmission, the widths of all units are set to 140 nm, and thus less than 0.84 dB insertion loss is maintained for each metalens. Meanwhile, the lengths of the units are modified to manipulate the wavefront as required by Equation (2). Two same metalens are formed into a 4-*F* system. By maximizing the reproduction (input to output) efficiency of the 4-*F* system, the actual focal length f (as labeled in Figure 1) is revealed to be 16.7 μm.

The MMS is then designed by changing the width and length of the units simultaneously to fulfill modulation requirements illustrated by Equation (1). To design the footprint of each unit in the MMS, proper weights are given to the transmission and phase, respectively, to search in the attained modulation library (Figure 2(D) and (E)) for the

best-matched slot width/length combination. Considering that the modulation range of the transmitted intensity is limited by the minimum feature size, a compromise has to be made to fulfill the demand for accurate computing in reality.

3 Simulation and experimental verification

To evaluate the performance of the designed device, an input-signal generator is involved to regulate the amplitude and phase in the waveguides, and thus a representative signal is generated. At the output, a sampling array composed of several single mode waveguides (500 nm width) is used to sample the results of the integrator. As for fabrication, the electron-beam lithography and inductively coupled plasma etching are used to transfer the designed pattern. Figure 3(A) presents an optical microscope image of the fabricated system and the inset is the zoom-in integrator as illustrated in Figure 1, together with the input and output waveguides.

Figure 3(B) shows the experimental setup. The light emitted from a laser is manipulated by the polarization beam splitter (PBS) and polarization controller (PC) before being coupled into the chip via a grating coupler, for better coupling efficiency. The output of each waveguide in the output-sampling array is coupled to a fiber by adjusting the coupling position. With the assistance of the beam splitter (BS), the results can be attained by the spectrometer and optical power meter simultaneously.

The simulated and measured (marked by hollow circles) results are provided and compared in Figure 3(C), as well as the theoretical output that is attained by calculating the numerical integration of incident light field. The inset presents the electric field (real part: Re (E)) distribution of the input signal. To be noted, only the intensity of light can be measured in the experiment, though the integrator is used to integrate the electric field. For comparison convenience, the simulated and theoretical results are presented in the form of light intensity as well. As only nine sampling waveguides are adopted, a dashed line is drawn to connect data points. All the curves are normalized. It is obvious that the simulated and experimental results fit well with theoretical ones in the paraxial region. In order to quantitatively evaluate the performance of the device, we define a similarity coefficient by referring to the coefficient of determination (R^2). The most general definition of the coefficient of determination is $R^2 = 1 - SS_{res}/SS_{tot}$, where SS_{res} and SS_{tot} denote residual sum of squares and total sum of squares, respectively. Calculation implies that $R^2_{sim-theory} = 83\%$ and $R^2_{exp-theory} = 78\%$ (for intuitive, "Sim" means simulation and "Exp" means experiment), showing that the proposed model performs well in both simulation and experiment.

To be noted, the deviations of the simulated and experimental outputs within main lobe owe to the fact that the high spatial-frequency components cannot be perfectly attenuated by the MMS, whose amplitude-modulation capability is limited by the minimum feature size of the lithography. Meanwhile, the side lobes may result from the difference between the ideal transmittance function $T(y)$ and the designed one $T'(y)$, leading to unfavorable modulations in low spatial-frequency region. One possible solution to this issue is to measure the low spatial-frequency components of the input signal individually, and use the results to compensate the output of the integrator [27]. As for the experimental output, its distribution

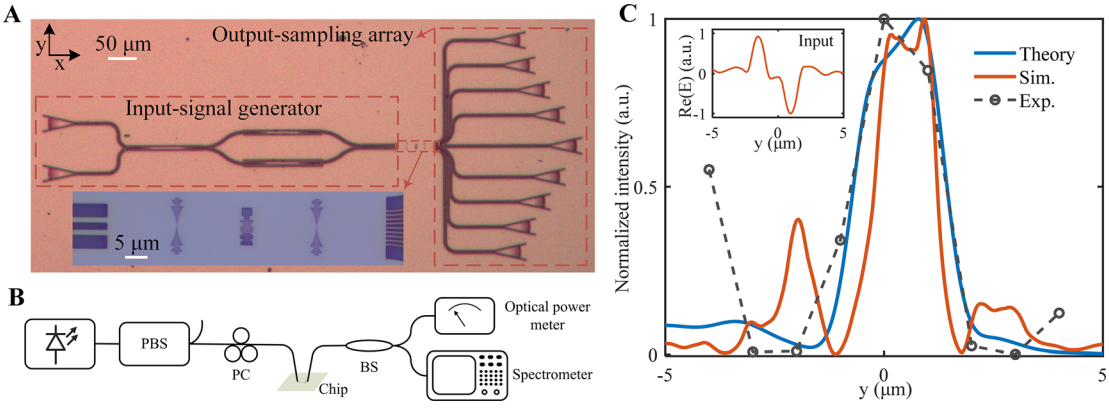

Figure 3: Experiments and results.
(A) Optical microscope images of fabricated schemes of fabricated on-chip integrator cascaded with input-waveguides and output-sampling array. (B) Experimental setup. (C) Comparison of simulated, experimental and theoretical results.

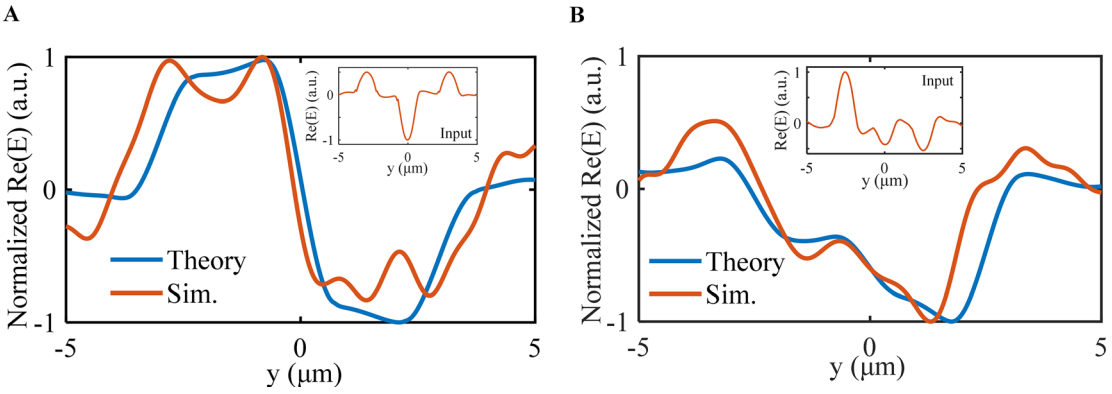

Figure 4: Comparison of simulated and theoretical results under incidences of (A) symmetrical and (B) asymmetrical input signals.

seems to be broadened compared with the simulated one, both for the width of main lobe and locations of the side lobes. This is supposed to be deviated from the fabrication error in lithography by affecting the practical focal length *f*. Furthermore, the fabrication error also affects the factual transmittance function of the MMS. On the other hand, the sampling period of the output waveguide array is limited to be 500 nm and the number of sampling points is restricted as well, and thus, the resolution is a compromise of crosstalk and accuracy.

To further investigate the feasibility of the integrator, more simulations are performed using different inputs. By tailoring the input signals, the outputs are simulated and then compared with theoretical ones in Figure 4(A) and (B). All the results are presented in form of Re*(E)* to better evaluate the performance. It can be noticed that the simulated results fit relatively well with theoretical curves. As for quantitative analysis, the similarity coefficients between the simulated and theoretical results are $R_A^2 = 83\%$ for Figure 4(A) and $R_B^2 = 67\%$ for Figure 4(B).

4 Conclusion

To conclude, we design, fabricate and characterize an on-chip optical integrator based on SOI platform. A novel symmetry-slot structure is introduced to form three metasurfaces in a 4-*F* system. The footprint of the integrator is 66.8 by 14 μm. The proof-of-concept experiment proves that the measured output light field is well in alignment with the theoretical distribution, with the similarity coefficient of 78%. As a basic operation in the AOC, this integrator has the merit of ultra-high speed, ultra-low power consumption and parallel-computing capability. Moreover, other devices such as convolver, differentiator and equation solver can be realized easily by modifying the MMS.

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