Research article

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Plasmonic electro-optic modulator based on degenerate semiconductor interfaces

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Abstract: We present a semiconductor-based optoelectronic switch based on active modulation of surface plasmon polaritons (SPPs) at lattice-matched indium gallium arsenide ($In_{0.53}Ga_{0.47}As$) degenerately doped pn^{++} junctions. The experimental device, which we refer to as a surface plasmon polariton diode (SPPD), is characterized electrically and optically, showing far-field reflectivity modulation for mid-IR wavelengths. Self-consistent electro-optic multiphysics simulations of the device's electrical and electromagnetic response have been performed to estimate bias-dependent modulation and switching times. The numerical model shows a strong agreement with the experimental results, validating the claim of excitation and modulation of SPPs at the junction, thus potentially providing a new pathway toward fast optoelectronic devices.

Keywords: plasmonics; optoelectronics; semiconductor plasmonics; electro-optic modulator.

1 Introduction

The demand for ever faster information processing has led to enormous advances in the semiconductor industry and continuous progression towards smaller, faster, and more efficient electronic devices [1–3]. Despite the tremendous progress achieved, saturation in the microprocessor clock speed at about 3 GHz has been observed over the past few years [3–5]. Alternatively, optical interconnects possess an exceedingly high data carrying and processing capacity, which suggests that photonic devices have the potential to address some of the present bottlenecks in microprocessor technology [6–14]. However, dielectric waveguides and interconnects are limited by the fundamental law of diffraction, leading to dimensional mismatch between electronic and photonic components. Recently, the field of plasmotronics has been recognized as having the potential to merge optics and electronics, in effect paving the path for a new era of fast data communications and computing in which both optical and electronic signals can be controlled simultaneously [15–17]. Furthermore, plasmotronics promises devices with ultra-small spatial footprints and ultrafast operating speeds [18–37]. This is accomplished through the excitation of localized particle surface plasmons (PSPs) or propagating surface plasmon polariton (SPP) waves [38]. In particular the SPPs are typically transverse magnetic (TM) waves that can be excited at the interfaces of metals or highly doped semiconductors. A separate type of SPPs that are transverse electric (TE) in nature can also exist at the interfaces involving artificial materials with negative permeability. SPPs' unique spatial confinement makes them ideal for the development of optical devices with spatial dimensions much smaller than those of traditional optical counterparts and thus more compatible with current nanosized electronic devices. Use of electromagnetic waves as signal carriers may also provide a dramatic speed-up in performance, as photons are not constrained by inertia as is the case with charges in electronic circuits.

In the past decade, substantial efforts have been invested in demonstrating the synergy between electronics and metal-based plasmonics. These efforts have stimulated a host of novel developments in plasmonic-based optoelectronic elements, such as an all-optical limiter [39], and waveguiding and switching [40–46]. Surface plasmon modes in low-dimensional cavities have been shown theoretically to serve as excellent sources of radiation with 3 dB bandwidths surpassing 1 THz [18]. All-optical

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absorption and gain-assisted switching has been demonstrated using an SPP waveguide, a Au film coated with a PMMA (poly(methyl methacrylate)) layer [28], and a cavity filled with a semiconductor (InGaAsP) gain material [47]. Metal-oxide-Si field-effect plasmonic modulator and all-optical modulation by plasmonic excitation of CdSe quantum dots have been investigated at visible and telecommunication frequencies [21, 22]. Recently, a fast all-optical switch based on a carbon nanotube metamaterial has been proposed, but the device showed a rather low transmission modulation of less than 10% [23]. Switching of SPPs has been also investigated on metal-dielectric surfaces using thermo-optical effects in polymers [48–50], semiconductor-loaded plasmon waveguides [51–53], and corrugated semiconductors [54, 55]. The SPP modulation rates so far demonstrated range from a few kHz [21] to tens of MHz [44–46] and into the GHz range [56, 57].

Despite the above-described progress, metal-based plasmonics have a few shortcomings such as fixed plasma frequency, and thus limited SPP operation frequency range, as well as possible challenges with integration within the current complementary metal-oxide-semiconductor (CMOS)-based technology. An alternative approach is to develop semiconductor-based plasmonic devices. Within this framework, degenerately doped semiconductors represent one promising alternative to metals, as their plasma frequency (i.e. the frequency marking the onset of "metallic" behavior) can be controlled by doping and/or carrier injection; therefore, such semiconductors represent a class of tunable high-quality materials for the field of plasmonics. In addition, semiconductor plasmonics benefits from advanced microelectronics fabrication technologies that have been developed over the past 50 years. Thus, optoelectronic and all-optical devices based on semiconductor plasmonics can offer a unique solution toward merging subwavelength optics with nanoelectronics.

In this work, we build upon our original proposal of a highly doped (degenerate) semiconductor-based optoelectronic switch referred to as a surface plasmon polariton diode (SPPD) [58–60]. Specifically, we present an important step toward realizing such a device by experimentally demonstrating for the first time excitation and modulation of SPP modes at degenerate lattice-matched indium gallium arsenide ($In_{0.53}Ga_{0.47}As$) pn^{++} junctions grown epitaxially on indium phosphide (InP). Electrical and optical characterization of the device is performed, unambiguously demonstrating coupling-, external bias-, and wavelength-dependent modulation (switching) of SPP modes at the pn^{++} junction. Also, to further enhance our understanding of the SPPD operation principles, we employ an electro-optic multiphysics numerical model, which self-consistently solves the Maxwell's, Poisson-Boltzmann, and drift-diffusion equations. This model allows accurate simulations of the excitation and electro-optical control of the SPPs, local electron and hole carrier transport across the pn^{++} junction, and the spatial- and time-dependent local permittivity variations as a function of external bias and wavelength. Under steady-state operation, close agreement is achieved between theory and experiment, indicating the potential of the presented device architectures as an excellent optoelectronic switch. Furthermore, using the numerical model we have performed time-dependent studies indicating that the current device architecture is capable of operating at data rates up to 1 Gbit/s, while scaling down the device size can further improve the data rate up to 50 Gbits/s. The experimental validation of the SPPD's temporal response will be a subject of a future study.

2 SPPD: fabrication and experimental setup

The basic schematic of the $In_{0.53}Ga_{0.47}As$-based SPPD under consideration is shown in Figure 1. It consists of a highly p-doped layer and a degenerately doped n^{++} layer grown on InP with an active drift-diffusion region formed between the top grating electrode (anode) and side contact (cathode). The operational principle of the devices is as follows: Under zero external bias, the state of the device is 'ON' supporting the excitation and propagation of the SPP modes at the pn^{++} junction. The SPP modes

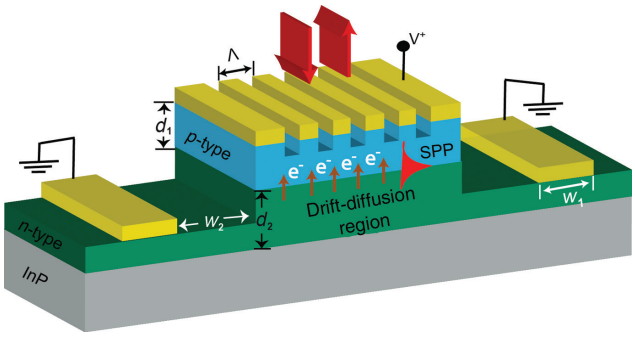

Figure 1: Basic schematic of the surface plasmon polariton diode (SPPD).
The SPPD consists of a lattice-matched indium gallium arsenide ($In_{0.53}Ga_{0.47}As$) pn^{++} junction grown epitaxially on an indium phosphide (InP) substrate. A grating with period $\Lambda = 2.4$ μm is used to couple mid-IR incident light to the surface plasmon polariton (SPP) modes propagating the junction interface. The relevant device sizes are as follows; $d_1 = 0.75$ μm, $d_2 = 1$ μm, $w_1 = 100$ μm, and $w_2 = 50$ μm.

are coupled from external TM radiation via a grating with period $\Lambda = 2.4$ μm. In the presence of a forward voltage bias V, electrons are injected from the n^{++}-doped layer into the p-doped layer, thus altering the p-layer permittivity ϵ_p. Under sufficiently high bias, $V > V_c$, where V_c is a critical voltage, the p-layer can acquire metal-like characteristics. As a result, the propagation of the SPP modes within the active drift-diffusion region is hindered, corresponding to the "OFF" state of the device. The critical voltage for a given operational frequency ω_o is given as $V_c = \frac{k_B T}{q} \ln[\varepsilon_b \omega_o^2 / \omega_{pp}^2]$, where $\omega_{pp} = q n_i / \sqrt{\varepsilon_b m_e N_A}$ is the plasma frequency of the minority carriers in the p-layer under thermal equilibrium, m_e is the electron's effective mass, ε_b is the contribution of the lattice electrons to the semiconductor permittivity, and n_i and N_A are the intrinsic and the acceptor doping concentrations [61].

The fabrication steps leading to the SPPD geometry shown in Figure 1 are depicted in Figure 2. The $In_{0.53}Ga_{0.47}As$-based pn^{++} junction device fabrication involves standard UV lithography, dry etching, and metal deposition. A degenerately doped pn^{++} junction was grown by molecular beam epitaxy with doping concentrations $N_A = 1 \times 10^{18}$ cm^{-3} and $N_D = 3.4 \times 10^{19}$ cm^{-3}. A hard mask was made by first depositing approximately 640 nm of silicon nitride (SiN_x) using plasma-enhanced chemical vapor deposition (PECVD, $NH_3/N_2/SiH_4$, 10/500/40 sccm). The SiN_x was then fabricated into mesa patterns (1200 μm × 1000 μm) via standard UV photolithography and dry etching (CHF_3/O_2, 20/4 sccm). The patterned SiN_x served as a hard mask for the device mesas, formed on the InGaAs sample using inductively coupled plasma (ICP) dry etching ($Cl_2/CH_4/H_2$, 6/4/7 sccm) with an etch depth of approximately 1300 nm. A buffered oxide etcher (BOE) solution was then used to remove the SiN_x hard mask. A 350-nm-thick SiN_x electrical isolation layer was then defined on top of the mesa structures with a second PECVD deposition, lithography, and dry etch. Both the bottom and top contact layers were then fabricated by UV photolithography, metal deposition (Ti/Au, 10/250 μm), and lift-off. The top contacts were aligned so that the bonding pad sits above the SiN_x isolation layer, with the gratings extending onto the top of the $In_{0.53}Ga_{0.47}As$ mesa. Next, grating structures in the p-$In_{0.53}Ga_{0.47}As$ layer were

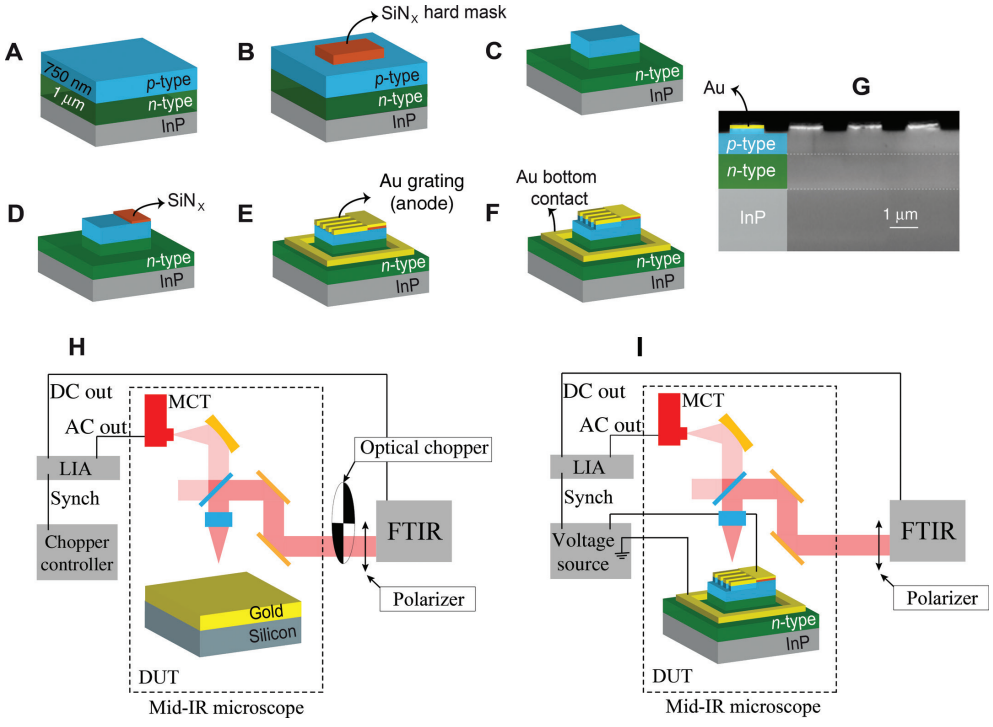

Figure 2: SPPD fabrication, sample SEM image, and experimental setup.
(A) Layer structure of the $In_{0.53}Ga_{0.47}As$ pn^{++} diode grown on InP. (B) Device layout after first SiN_x deposition and fabricated into mesa patterns. (C) ICP dry-etching to form a mesa pattern on the p-doped layer, followed by BOE etching to remove SiN_x. (D) Second SiN_x deposition into an electrical isolation layer. (E) Bottom and top metal contact deposition. (F) ICP dry-etching of grating. (G) Cross-sectional SEM image of the device. Experimental setups for (H) obtaining the reference gold surface reflection and (I) polarization-dependent reflection change under external applied voltage.

dry etched ($Cl_2/CH_4/H_2$, 6/4/7 sccm), with an etch depth of ~120 nm into the p-$In_{0.53}Ga_{0.47}As$. As this etch used the top Ti/Au grating structure as the etch mask, this step also removed ~100 nm of the Au grating. All other regions of the sample were protected by photoresist during the grating etching process and were later cleaned by oxygen plasma. Schematics of the initial wafer and the device structures at each stage of the fabrication step are shown in Figure 2A–F. Figure 2G shows the scanning electron microscopy (SEM) cross-sectional image of the device. The samples were then mounted on copper blocks with indium paste and wire-bonded to ceramic stand-off pads.

Upon fabrication, the SPPD is characterized through polarization-dependent reflectivity measurements using a Bruker v80V Fourier transform infrared (FTIR) spectrometer working in fast-scan mode and normalized to reflection of a gold surface (see Figure 3A, solid lines). To measure the polarization-and voltage-dependent change in reflectivity, we used the setups shown in Figure 2H, I. First, we set the Bruker v80V FTIR spectrometer to operate in the amplitude-modulation step-scan mode; next the incident light from the FTIR is sent through a polarizer and then through an optical chopper. The optical chopper modulates the light entering an infrared microscope (Bruker IR1). The incident, modulated light is focused onto the gold surface using the microscope's Cassegrain objective (15×), and the reflected light from the gold surface is collected by the same objective and focused onto the microscope's internal HgCdTe (MCT) detector. The output from the detector was then sent to a lock-in amplifier (LIA) that is synchronized to the optical chopper frequency and demodulated, with the DC output of LIA fed into the FTIR and recorded at each mirror position giving the reflection spectrum of the gold surface. To measure the polarization- and voltage-dependent change in far-field reflection spectrum of the device, the experimental setup is same as described above, except that the optical chopper is removed and the gold surface sample is replaced by the final grating device (see Figure 2I). The external bias to the grating sample is applied using a pulse generator outputting a square wave voltage signal with amplitude V at 10 kHz. The detector output is then fed into the LIA, which is set to be synchronized to the pulse generator, allowing for measurement of the change in reflection. The change in reflection is mainly attributed to electron injection from n^{++} layer into the p layer in the presence of an external

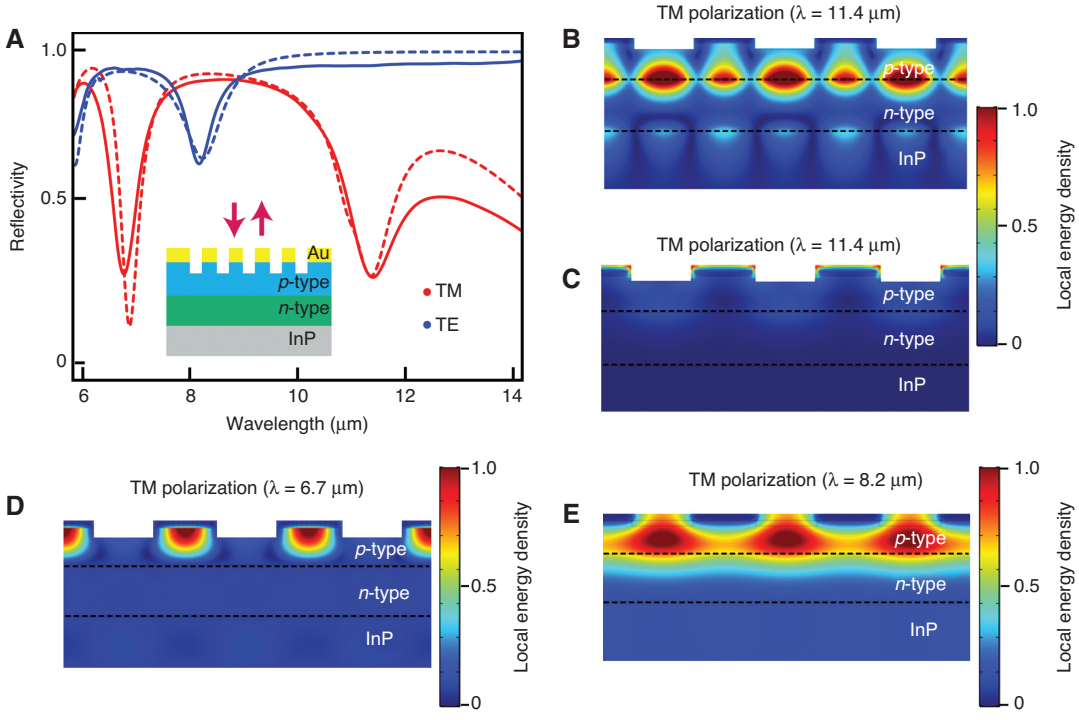

Figure 3: SPPD reflectivity spectra and local electromagnetic mode profiles.
(A) Transverse magnetic (TM) and transverse electric (TE) polarized reflectivity spectra of the $In_{0.53}Ga_{0.47}As$ grating device (see insert) under zero bias. The experimental data (solid lines) is compared with self-consistent electro-optic simulations (dashed lines).
The local electromagnetic energy densities across the device for the two incident light polarizations: (B–D) Transverse magnetic (TM) and (C, E) transverse electric (TE). The electromagnetic mode profiles unambiguously shows the excitation of SPP at the pn^{++} junction interface for incident TM radiation with free-space wavelength of $\lambda = 11.4$ μm.

forward bias. Finally, the obtained spectrum is normalized to the reflection from the gold surface, which yields an absolute change in reflectivity (ΔR).

3 Forward-bias-assisted SPP modulation

Figure 3A shows the TE and TM polarization reflectivity spectra of the unbiased SPPD. The reflectivity spectra for the TM-polarized light shows distinctive dips at $\lambda \sim 6.7$ μm and $\lambda \sim 11.4$ μm, whereas when TE-polarized light is incident upon the device, a dip in reflectivity is observed at $\lambda \sim 8.2$ μm. To investigate the electromagnetic modes supported by the device corresponding to each reflection dip position, we proceeded to numerically characterize the fabricated $In_{0.53}Ga_{0.47}As$-based SPPD. For this, first the device under zero external bias is studied. The pn^{++} junction characteristics such as junction depth, electron and hole mobilities, relaxation rates, and doping concentrations have been already extracted in our previous work [60]. These device characteristics were then used in the developed COMSOL-based electro-optic model [58, 59]. The multiphysics model self-consistently solves for the charge transport and electromagnetic response in the absence and presence of external bias. The COMSOL semiconductor module (CSM) provides the local electron $n(\vec{r}, V)$ and hole $p(\vec{r}, V)$ concentrations across the junction, which are then used to estimate the inhomogeneous dielectric function in all regions of the device. In the simulations, an inhomogeneous Drude model is implemented to describe the permittivities including both the electron and hole contributions: $\varepsilon(\omega, \vec{r}) = \varepsilon_b - \omega_{pn}^2(\vec{r}) / (\omega^2 + i\omega\omega_{\tau n}) + \omega_{pp}^2(\vec{r}) / (\omega^2 + i\omega\omega_{\tau p})$, where $\varepsilon_b = 11.64 + i0.15$ is the permittivity of the bound electrons in the mid-IR frequency range. The position- and bias-dependent electron and hole plasma frequencies, $\omega_{pn}(\vec{r}, V) = \sqrt{q^2 n(\vec{r}, V) / \epsilon_0 m_e}$ and $\omega_{pp}(\vec{r}, V) = \sqrt{q^2 p(\vec{r}, V) / \epsilon_0 m_h}$, are obtained from the local carrier densities (n and p), while the relaxation frequencies $\omega_{\tau n} = q/(m_e \mu_n(N_A, N_D))$ and $\omega_{\tau p} = q/(m_h \mu_p(N_A, N_D))$ are dependent on the doping concentrations through the corresponding mobilities. The obtained electromagnetic parameters are finally used in the COMSOL electromagnetic module (CEM) to obtain both TE and TM reflectivities of the device.

A comparison between the experimentally and numerically obtained reflectivity spectra is presented in Figure 3A. The observed dip in the TM reflectivity at $\lambda \sim 11.4$ μm is attributed to the excitation of SPP at the pn junction, while the dips in the TM reflectivity at $\lambda \sim 6.7$ μm and TE reflectivity at $\lambda \sim 8.2$ μm correspond to Fabry-Perot resonances in the dielectric p layer. This is clearly seen in Figure 3B–E, where we show the local electromagnetic energy density across the device. As expected, only in the case of TM polarization and at $\lambda \sim 11.4$ μm do we observe an SPP mode propagating at the pn^{++} junction interface (see mode profiles in Figure 3B), while no such mode exists in the case of TE polarization (see Figure 3C). The SPP is excited by the grating and exponentially decays within the p and n^{++} regions. To the best of our knowledge, this is the first experimental demonstration of SPPs at semiconductor junctions at mid-IR frequencies. The mode profiles depicted in Figure 3D and E are localized entirely within the p layer and do not have SPP characteristics; instead, they are typical Fabry-Perot resonances formed between the n-doped layer and the top grating electrodes.

To assess the SPPD signal modulation, we have performed reflectivity studies under applied forward voltage bias. The numerical (dashed line) and experimental (solid lines) results are depicted in Figure 4, where we plot the absolute change in reflectivity $|\Delta R(\lambda, V)| = |R(\lambda, V) - R(\lambda, 0)|$ for a set of forward voltages. Here, we restrict our studies for a wavelength window centered around the SPP coupling wavelength ($\lambda = 11.4$ μm) for added clarity. As the external forward bias is increased, a far-field reflectivity modulation with respect to the unbiased device is observed. This behavior is consistent with expectations and is revealed both in the experimental data and numerical results. The SPP modulation is due to the

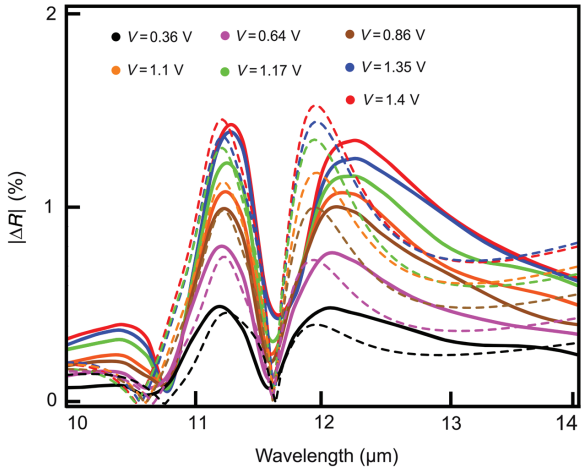

Figure 4: SPPD reflectivity modulation under external voltage bias. The absolute change in reflectivity is experimentally obtained under various forward bias voltages (solid lines) and compared with the self-consistent electro-optic simulations (dashed lines).

significant increase in the minority carrier concentration within the device's p layer, which alters the local permittivity, eventually leading to switching off the SPPs at the junction. While the correspondence between theory and experiment is good, a discrepancy is observed for higher wavelengths ($\lambda > 13$ μm). Our simulations show that this deviation is probably due to a wavelength-dependent permittivity ε_b of the bound electrons, which in our model was set to a constant value. Finally, we should point out that the observed far-field reflectivity modulation of $\Delta R \approx 1\%$ is rather low. The reason is the way we collect the "signal", that is, the reflected light coming from the entire device including the top metal electrodes. Correspondingly, the modulation of the far-field reflectivity only indirectly represents the changes in the SPP's propagation properties at the junctions. Since the purpose of this study was to present a proof of concept only, this indirect scheme was chosen because of its simplicity. Better schemes based on matching in-coupling and out-coupling gratings that can allow a direct measure of the SPPs signal will be subject of future studies.

4 SPPD response time: numerical simulations

In our earlier theoretical studies [58, 59] we have shown that semiconductor-based SPPDs can provide excellent switching rates. To assess the response times of the experimental device, we have used the already validated self-consistent electro-optic model [60] and performed a transient analysis under the input voltage biases used in the reflectivity studies (see Figure 4). When performing the simulations, we operate the device at the two incident wavelengths corresponding to the two major peak positions ($\lambda = 11.2$ μm and $\lambda = 12$ μm) in the reflectivity spectra (see Figure 4). The obtained results under a step-type input are shown in Figure 5. As the SPPD is forward-biased, the far-field reflectivity is modulated corresponding to SPP switching off. The modulation of the signal increases with increasing bias. A well-defined distinction between the OFF and ON rise/fall times is observed, with the latter being substantially faster. This distinction can be attributed to the significantly different physical mechanisms that are involved when the device is under forward and zero bias. Close inspection reveals that the OFF times are governed predominantly by the time of flight of minority carriers (electrons) across the pn^{++} depletion region, while the ON times are facilitated by charge diffusion and recombination in the quasi-neutral regions. Furthermore, the SPP modulation rates are revealed to be slightly dependent on the operation frequency.

To better assess the SPPD switching rates we have performed extensive studies of the 3-dB ON (τ_{3dB}^{ON}) and OFF (τ_{3dB}^{OFF}) times. The extracted response times as function of the applied bias and for the two different incident wavelengths are shown is Figure 6. Close inspection reveals that the OFF times are inversely proportional with the applied external bias for $V < V_c = 0.87$ V, and saturate at $\tau_{3dB}^{OFF} \approx 0.5$ ns for $V > V_c$. This is because the electron injection rate into the p layer is proportional to the applied bias. The ON times are weakly dependent on the external bias. This is due to the fact that the excess minority carriers in the p layer are removed by net outflow from the quasi-neutral region by the process of diffusion and charge recombination. This distinctive behavior can be quantitatively explained using a simple drift-diffusion

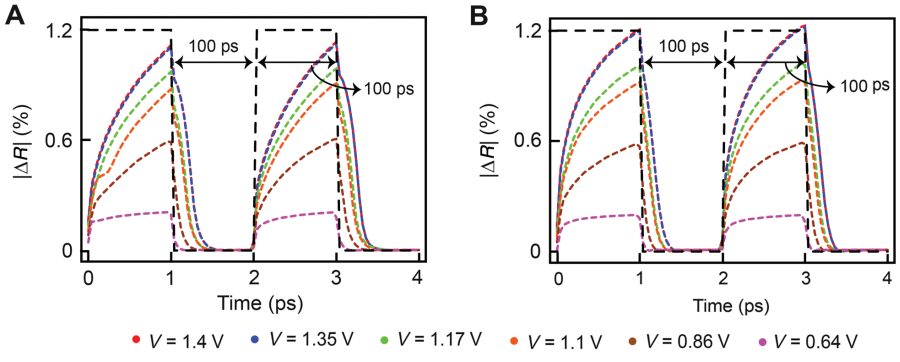

Figure 5: SPPD switching.
Far-field absolute change in reflectivity (dashed lines) under step-type input voltage (dashed black line) under various forward bias voltages. The signal is repetitively switched following the external voltage. In the calculations the operation wavelength is set at (A) $\lambda = 11.2$ μm and (B) $\lambda = 12$ μm.

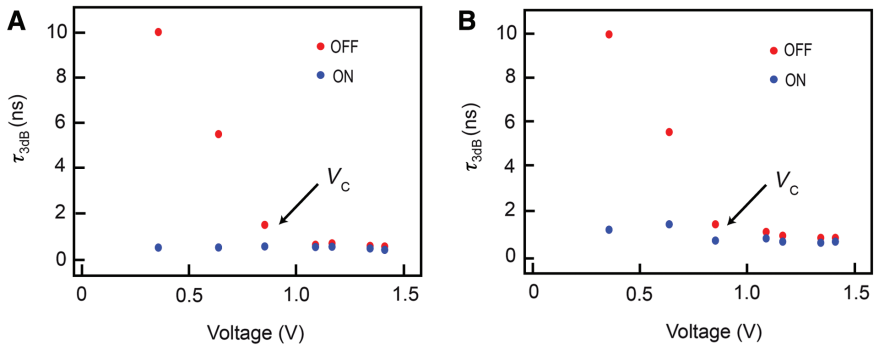

Figure 6: SPPD response times as function of the applied external bias.
In the calculations, the operation wavelength is set at (A) $\lambda = 11.2$ μm and (B) $\lambda = 12$ μm.

model of the electron concentration dynamics in the drift-diffusion region [58, 59]. Overall, our data shows that for sufficiently high applied voltages, 3-dB data rates in excess of 1 Gbit/s can be achieved. However, operating the SPPD at high applied voltages will inevitably result in ohmic heating and increase in the device local temperature. These temperature effects have been already studied in [59], where we have showed that restricting the voltage to $V \approx V_c$ leads to acceptable temperature rise of less than 10 K. Finally, it should be noted that the current work serves as the proof of concept and to the best of our knowledge the first experimental demonstration of SPP's excitation and modulation at highly doped pn^{++} junction. Further improvement in the reflectivity modulation, switching rates, and minimization of the power dissipation is expected by reducing the size of the SPPD drift-diffusion region (see Figure 1) and varying the p and n^{++} layer doping concentrations while keeping the SPP operation frequency within the mid-IR spectral range. The potential for substantial improvement in performance has been already studied theoretically in our previous work [59], where we have shown that optimal SPPD device architectures can lead to data rates in excess of 50 Gbits/s. The experimental realization of such optimal device will be the subject of future studies.

5 Conclusion

In conclusion, we have fabricated and electrically and optically characterized an SPPD based on lattice-matched $In_{0.53}Ga_{0.47}As$ degenerate pn^{++} junction. For a first time, the excitation of SPPs at degenerate semiconductor interfaces and within the mid-IR frequency range has been demonstrated. The modulation of the SPP modes under the presence of an external forward bias was studied experimentally and compared with numerical simulations, validating the switching mechanism underlying the SPPD operation. The observed SPP modulation is the result of minority carrier injection across the metallurgical junction. Based on the excellent match between theory and experiment, we have performed time-dependent numerical studies of the SPPD response times under step-type input bias. Our theoretical results show that the current device architecture can support data rates of up to 1 Gbit/s, which can be further improved (up to 50 Gbits/s) with optimized geometries. Overall, the presented results indicate that SPP modes on degenerate semiconductor junctions can be utilized as signal carriers, which would be an important step toward the realization of fast optoelectronic circuit elements.

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Author contributions: RV, ZD, DW, and DG contributed equally in executing the idea, analyzing the data, and writing the manuscript. AB grew the material.

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