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#### Research article

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# Experimental demonstration of an optical Feynman gate for reversible logic operation using silicon micro-ring resonators

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Abstract: Currently, the reversible logic circuit is a popular research topic in the field of information processing as it is a most effective approach to minimize power consumption, which can achieve the one-to-one mapping function to identify the input signals from its corresponding output signals. In this letter, we propose and experimentally demonstrate an optical Feynman gate for reversible logic operation using silicon micro-ring resonators (MRRs). Two electrical input signals (logic operands) are applied across the micro-heaters above MRRs to determine the switching states of MRRs, and the reversible logic operation results are directed to the output ports in the form of light, respectively. For proof of concept, the thermo-optic modulation scheme is used to achieve MRR's optical switching function. At last, a Feynman gate for reversible logic operation with the speed of 10 kbps is demonstrated successfully.

**Keywords:** integrated optics; optical switching devices; optical logic devices; resonators; photonic integrated circuits.

# 1 Introduction

Nowadays, traditional Boolean computers composed of field-effect transistors (FETs) are based on irreversible

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logic operations. Generally, these computers achieve a very large-scale integration of 10° transistors per chip with the further improvement of their performances, which will induce the heat-dissipation problem. Landauer [1] ever elaborated that each bit of information loss generates kTln2 joules of heat energy for traditional irreversible logic computation, where k is the Boltzmann constant, and T is the absolute temperature. The amount of heat dissipation for the loss of each bit of information is small  $(\sim 2.9 \times 10^{-21} \text{ J})$ , but not negligible as the total amount of heat dissipation is very considerable when the great amount of information data is needed to process. The reversible logic scheme can achieve a one-to-one mapping function to identify the input signals from its corresponding output signals, which means each input signal determines a unique output signal, and each output signal can also trace a unique input signal. The one-to-one mapping function makes it possible to restore the inputs from the outputs without energy consumption and information loss. Therefore, the reversible logic does not wipe any information while avoiding the dissipating heat, which is very important for the future high-speed information processing.

Currently, various reversible logic circuits have been proposed and demonstrated based on different schemes in order to solve the heat-dissipation problem induced by the loss of a bit of information, such as spatial light scheme [2], fiber-based scheme [3], photon quantum scheme [4–10], and chemistry and biology scheme [11–13]. However, all these schemes are not compatible with the commercial complementary metal-oxide-semiconductor (CMOS) in fabrication process, and they are also inconvenient in achieving large-scale integration, which can induce high fabrication cost and limit their applications in the field of on-chip information processing. Therefore, it is necessary for us to find a novel scheme to achieve reversible logic operations with low fabrication cost, high operation speed, and mature fabrication process using the new media and technology.

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Recently, silicon photonics, in which laser, optical modulator, photon detector, optical switch, etc., are integrated on a small silicon chip to achieve the functions of information processing, has attracted more and more attention from academic communities due to its nature such as parallelism, high operation speed, high bandwidth, large-scale integration, CMOS-compatible fabrication process, and low cost [14, 15]. Therefore, it is a most promising scheme for us to achieve optical reversible logic operations using silicon photonics technology. In fact, diversified silicon-based optical logic devices have been proposed and experimentally demonstrated during the past years [16–20]; however, most of them still belong to traditional irreversible logic schemes in which the heat dissipating is inevitable [1]. In this letter, we propose and demonstrate an optical Feynman gate for reversible logic operation based on silicon micro-ring resonators (MRRs) using the commercial CMOS fabrication process. As we know, silicon MRR is a most promising building block for silicon-based integrated photonic devices due to its compact size, low power consumption, and high response speed [21, 22]. Therefore, compared with Refs. [5] and [6], the proposed Feynman gate based on MRRs has many advantages such as compact size, high operation speed, large scale integration, and low fabrication cost, etc.

## 2 Results and discussion

The Feynman gate has two inputs (X, Y) and two outputs (A, B), which can achieve reversible logic operations. The output signals are determined by the function A=X and  $B = X \oplus Y$ . The schematic of the Feynman gate composed of two cascaded MRR switches and a 1×2 MMI coupler is shown in Figure 1A. The five ports of the device are defined as Input, Control port, Target port, Through1, and Through based on their specific functions. The twoinput Feynman gate is also called the Controlled-NOT gate (CNOT), and its truth table is shown in Table 1, from which we can easily identify any input or output based on its assigned counterpart. In other words, the output signals achieved by the proposed device are corresponding to the input signals by one-to-one.

The working principle of the proposed device can be summarized as follows: a monochromatic continuous optical wave with a working wavelength of  $\lambda_w$  is coupled into the input port of the device, and the propagation path of the optical wave is controlled by two independent electrical pulse sequences (EPS) X and Y applied on the microheaters above MRR, and MRR, respectively. The low and high levels of the electrical pulse sequences are defined as

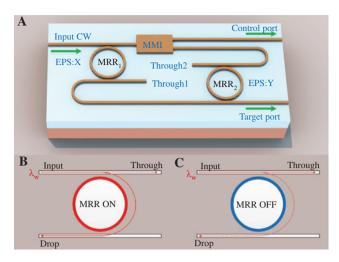


Figure 1: Schematic of the proposed device and switching element. (A) Schematic of the proposed optical Feynman gate (CW, continuous wave; MRR, micro-ring resonator; EPS, electrical pulse sequences; MMI, multimode interference coupler), the control port can implement the function A = X and the target port can implement the function  $B = X \oplus Y$ . Configurations of MRR-based switching element at (B) ON state and (C) OFF state.

**Table 1:** The truth table achieved by the proposed device.

х	Υ	Control port	Target port
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

logic 0 and 1 in the electrical domain. Meanwhile, the low and high levels of the optical power detected at the Control port and Target port represent logic 0 and logic 1 in the optical domain. We define that each MRR is ON-resonance at  $\lambda_w$  when the applied voltage is at low level (logic 0), and then the light can be downloaded to the drop port of MRR (Figure 1B). On the contrary, MRR is OFF-resonance when the applied voltage is at high level (logic 1), and then the light is directed to the through port without disturbances (Figure 1C). Based on the working mode definition of MRR, when the voltages applied to MRR, and MRR, are both at the low level (X=0, Y=0), the light with the working wavelength of  $\lambda_{w}$  coupled into the device is downloaded by MRR, and MRR, successively, and the light is directed to the Through2 port at last (Figure 1A). Therefore, the optical power at the Control and Target ports are both at the low level (Control port = 0, Target port = 0). When the voltages applied to MRR, and MRR, are at the low and high levels (X = 0, Y = 1), respectively, the optical wave is downloaded by MRR, first, and then bypasses MRR, directly.

The light is directed to the Target port at last. It is obvious that the optical power is at low level at the Control port and high level at the Target port (Control port = 0, Target port = 1). When the voltages applied to MRR, and MRR, are at high and low levels (X = 1, Y = 0), respectively, the optical wave bypasses MRR, directly, and then, it is divided into two parts by the MMI coupler. Subsequently, half of the optical wave is directed to the Target port by MRR, and the remaining optical wave is directed to the Control port simultaneously. Thus, the optical powers are both at the high level at the Control and Target ports (Control port = 1, Target port=1). When the voltages applied to MRR, and MRR, are both at high levels (X = 1, Y = 1), the optical wave bypasses MRR, first, and then, it is divided into two parts by the MMI coupler; after that, half of the optical wave bypasses the MRR, and propagates to Through2. In the remaining optical wave, half of the light is directed to the Control port simultaneously. The optical power exhibits a low level at the Control port and a high level at the Target port (Control port = 1, Target port = 0). Based on the above elaboration, the truth table shown in Table 1 can be achieved by the proposed device. From the above discussion, it is clear that the proposed logic circuit can perform the reversible logic operations of two bits, and there is a one-to-one function to identify input signals from their corresponding output signals.

The device is fabricated on a silicon-on-insulator (SOI) wafer with a 220-nm-thick top silicon layer and 2-µm-thick buried SiO<sub>2</sub> layer using the commercial CMOS fabrication process. The optical waveguide with 400 nm in width, 220 nm in height, and 90 nm in slab thickness is used to construct the circuit, which only supports the quasi-TE fundamental mode. The radii of MRRs are both 10 µm, all the gaps between ring waveguides and straight waveguides are 400 nm (Figure 2B and C). Spot size

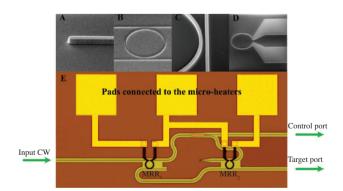


Figure 2: Scanning electronic micrograph (SEM) of (A) the spot size converters (SSC), (B) the parallel MRR, (C) the gap between ring waveguide and straight waveguide, and (D)  $\Omega$ -shaped TiN microheater. (E) Micrograph of the fabricated optical Feynman gate.

converters (SSCs) are integrated on the terminals of the circuit in order to improve the coupling efficiency between the device and input/output lensed fiber (Figure 2A). Two  $\Omega$ -shaped TiN micro-heaters with widths of 2  $\mu$ m are fabricated on the top of ring waveguides in order to tune MRRs by thermo-optic effect (Figure 2D). Finally, the aluminum trances are sputtering to connect the TiN micro-heaters and the 80×80 µm<sup>2</sup> pads. The microscope image of the fabricated device is shown in Figure 2E.

An amplified spontaneous emission source (ASE), two tunable voltage sources (TVS), and optical spectrum analyzer (OSA) are first employed to characterize the static response of the device. Meanwhile, the working wavelength and voltages of each electrical pulse sequence are determined by the device's static characterization. Broadband light generated by ASE is coupled into the input port of the device through a lensed fiber, and the output light is fed into the OSA through another lensed fiber. Two TVSs are employed to tune two TiN micro-heaters above the corresponding MRRs, respectively. The static response spectra at the Control port are shown in Figure 3A-D, and the static response spectra at the Target port are shown in Figure 4A-D.

The resonant wavelength of MRR, is shorter than that of MRR, due to the limited fabrication accuracy. At first, a pre-bias of 0.55 V is applied to MRR, to compensate the fabrication error and guarantee that two MRRs have the same resonant wavelength at the original state (X=0,Y = 0) (Figure 3A). The wavelength of 1546.22 nm is chosen as the working wavelength.

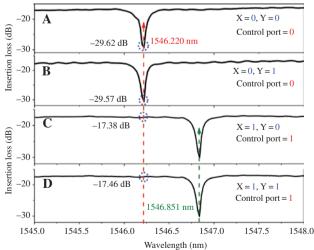
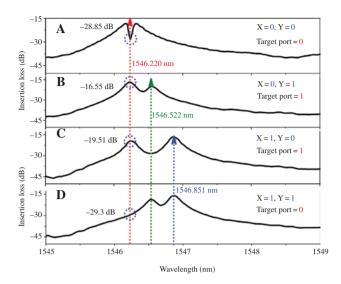
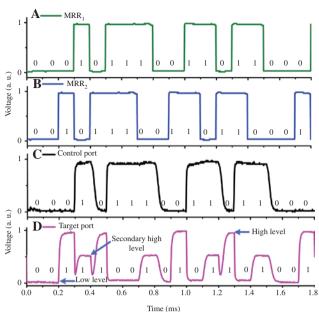


Figure 3: Response spectra of the device at the Control port with the applied voltages to the micro-heaters over MRR,, MRR,, being (A) 0 V and 0.55 V, (B) 0 V and 1.71 V, (C) 1.93 V and 0.55 V, (D) 1.93 V and 1.71 V.



**Figure 4:** Response spectra of the device at the Target port with the applied voltages to the micro-heaters over MRR<sub>1</sub>, MRR<sub>2</sub>, being (A) 0 V and 0.55 V, (B) 0 V and 1.71 V, (C) 1.93 V and 0.55 V, (D) 1.93 V and 1.71 V.

When the voltages applied to MRR, and MRR, through the TiN heaters are 0 V and 0.55 V, respectively (X = 0, Y = 0), there is a dip at 1546.22 nm due to the identical resonant wavelength of two MRRs. The optical wave is downloaded by MRR, and MRR, successively, and directed to the Through2 port at last; therefore, the optical powers at the Control port and Target port are both at a low level (Control port result = 0, Target port result = 0; Figures 3A and 4A). When the voltages applied to MRR, and MRR, are 0 V and 1.71 V (X = 0, Y = 1), respectively, the MRR, 's resonant wavelength shifts from its original location of 1546.22 nm to 1546.52 nm due to the thermo-optic effect. The optical wave is first downloaded by the MRR, and then bypassed MRR, and it is directed to the Target port at last. The optical power is at low level at the Control port and high level at the Target port (Control port result = 0, Target port result = 1; Figures 3B and 4B). When the voltages applied to MRR, and MRR, are 1.93 V and 0.55 V (X = 1, Y = 0), respectively, the MRR,'s resonant wavelength red-shifts which shift from its original location of 1546.220 nm to 1546.851 nm, due to the thermo-optic effect. The optical wave bypasses MRR, directly, and then, it is divided into two equal beams by the MMI coupler; afterward, half of the optical wave is downloaded to the Target port by MRR, and the remaining optical wave is directed to the Control port. Note that logical "1" has two different levels (the high level is about twice the secondary high level) for the device. Comparing Figure 4B with C, the corresponding phenomena also can be observed in the static response spectra (the insertion



**Figure 5:** Dynamic experiment results of this device. (A) Signals applied to MRR<sub>2</sub>, (B) signals applied to MRR<sub>2</sub>, (C) operation result of Control port, (D) operation result of Target port.

loss at the working wavelength of 1546.22 nm for Figure 4B is 3 dB higher than that for Figure 4C), but it does not influence the performance of the device as we can define the secondary high level as logical "1". According to the above discussion, the optical powers at the Control and Target ports are both at a high level in this working status (Control port result = 1, Target port result = 1; Figures 3C and 4C). When the voltages applied to MRR, and MRR, are 1.93 V and 1.71 V (X = 1, Y = 1), respectively, the optical wave bypasses MRR, first, and then, it is divided into two equal beams by the MMI coupler; after that, half of the optical wave bypasses MRR, and propagates to Through2. The remaining optical wave is directed to the Control port simultaneously. The optical power is at high level at the Control port and low level at the Target port (Control port result = 1, Target port result = 0, Figures 3D and 4D).

The dynamic response results of the device are shown in Figure 5. A continuous monochromatic optical wave at 1546.22 nm from a tunable laser is coupled into the Input port of the device through a lensed fiber. Two independent electrical pulse sequences at 10 kbps are applied to MRR $_1$  and MRR $_2$ , respectively (the low levels are 0 V and 0.55 V; the high voltage levels are 1.93 V and 1.71 V for MRR $_1$  and MRR $_2$ , respectively). The output optical wave is converted into an electrical signal by a photo-detector (PD). All the two input and output electrical signals are fed into a two-channel oscilloscope for waveform observation.

From Figure 5, we can obviously see that the 2-bit reversible logic operation of two electrical signals is achieved at the Control and Target ports, respectively. In addition, the function of the MMI coupler is as a power splitter; therefore, the optical power at the Target port in the working status ("01") is twice about that at the same port in the working status ("10"). However, it does not influence the performance of the device, and the detailed discussions are given in Ref. [18].

### 3 Conclusion

In conclusion, we propose and experimentally demonstrate an optical Feynman gate based on micro-ring resonators for a logically reversible operation with a speed of 10 kbps. There is a one-to-one function to identify inputs from the corresponding outputs, which will be beneficial to construct the "cool" computing. Next, the other advanced modulation schemes, such as the plasmadispersion effect or the electric field effect can be also employed to tune the MRR-based switch in order to further improve the operation speed of the device [18, 21, 22].

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**Competing interest:** The authors declare no competing financial interest.

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