Review article

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Progress in silicon platforms for integrated optics

Abstract: Rapid progress has been made in recent years repurposing CMOS fabrication tools to build complex photonic circuits. As the field of silicon photonics becomes more mature, foundry processes will be an essential piece of the ecosystem for eliminating process risk and allowing the community to focus on adding value through clever design. Multi-project wafer runs are a useful tool to promote further development by providing inexpensive, low-risk prototyping opportunities to academic and commercial researchers. Compared to dedicated silicon manufacturing runs, multi-project-wafer runs offer cost reductions of 100× or more. Through OpSIS, we have begun to offer validated device libraries that allow designers to focus on building systems rather than modifying device geometries. The EDA tools that will enable rapid design of such complex systems are under intense development. Progress is also being made in developing practical optical and electronic packaging solutions for the photonic chips, in ways that eliminate or sharply reduce development costs for the user community. This paper will provide a review of the recent developments in silicon photonic foundry offerings with a focus on OpSIS, a multi-project-wafer foundry service offering a silicon photonics platform, including a variety of passive components as well as high-speed modulators and photodetectors, through the Institute of Microelectronics in Singapore.

Keywords: silicon photonics; integrated optics; photonics platform; multi-project wafer shuttle.

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1 Introduction

In just the past few years, silicon has evolved into a functional platform for integrated optics [1, 2]. All of the basic building blocks of photonic systems, including waveguides [3, 4], modulators [5, 6] and detectors [7] have been demonstrated. Lasers are being integrated through a variety of mechanisms, ranging from bonding to epitaxy to package-level integration [8, 9]. The goal of producing complex integrated photonic circuits is quickly becoming the new reality.

The development of complex integrated photonic systems is where silicon will prove exceptional. As in electronics, photonic devices in silicon do not have the best performance relative to other material systems (although they have recently come very close in many areas). Instead, it is the ability to leverage complexity and build systems that gives silicon the advantage. To take advantage of the high yield and manufacturing infrastructure available in silicon, there are requirements in terms of device standardization and process stability. For systems development, having well-characterized and stable device performance and understanding the variance of key parameters is crucial. Additionally, a full silicon photonics process including modulators and detectors is prohibitively expensive for most research groups and small start-ups to develop on their own. High-resolution photomasks cost tens of thousands of dollars and a full silicon photonics platform can require 20 masks or more.

Similar issues existed for CMOS electronics in the late 1970s and early 1980s. The efforts led Carver Mead and Lynne Conway, among many others to develop the design methodology the dominates the microelectronics industry, where fabrication details are abstracted away into Process Design Kits (PDKs), allowing designers to move away from focusing on process integration issues. They also had a significant role in starting MOSIS (http://www.mosis.com), the first multi-project wafer (MPW) service. The advantage of multi-project-wafer services is that the costs of a wafer manufacturing run can be spread between a number of users [10] as shown in Figure 1. For the modest quantities that research requires, one-off costs such as those for masks usually dominate. MPWs can significantly cut the cost and development time needed to move an idea from the white board to a working prototype, and even into small-scale production.

Silicon photonics MPW services are now available, but the processes are still very much under development. This paper will cover the latest progress in developing such platforms, and will discuss some of the requirements and trends for the coming years in this area.

2 The silicon photonics platform

Over the past few years, silicon platforms have become available through foundry/MPW services. We will explore the devices offered in such platforms and the performance that can currently be achieved. The focus will be on the Optoelectronic Systems Integration in Silicon (OpSIS) MPW service at University of Delaware, which has developed a process using the Institute of Microelectronics (IME) foundry, a research institute of the Agency for Science,

Technology and Research (A*STAR) [11]. The OpSIS-IME foundry service is the only MPW process that has delivered silicon with a full active flow (passives, detectors and modulators). IME also offers a variety of processes directly to users. In Europe, ePIXfab (http://www.epixfab.eu/) provides access to a several different standardized photonics processes in collaboration with IHP, IMEC, and CEA-LETI. IHP offers a passives-only process on 220 nm SOI wafers (http://www.epixfab.eu/technologies/ihp-standard-passives). IMEC has three different platforms: simple 2-layer passives, advanced passives with poly-Si, and passives with modulators. CEA-LETI offers three platforms: passives only, passives with heaters, and passives with detectors. Both IMEC and CEA-LETI have recently announced that they plan to offer fully integrated platforms through ePIXfab later this year [12].

There are a number of similarities between the different foundry offerings. All four foundry platforms mentioned above have standardized on an 8-inch SOI wafer with a 220 nm device layer and a 2 µm buried oxide (BOX) layer. The processes use 248 nm (IME, IHP) or 193 nm (IMEC, LETI) lithography to define the layers. Anisotropic etch steps are employed to define various layers in the silicon as shown in Table 1, and ion implantation into silicon allows formation of junctions.

Apart from the silicon etches, there are a number of distinctions between the platforms. The IMEC process offers a poly-silicon layer to enhance grating coupler efficiency. The full flow and detector processes all offer selectively grown epitaxial germanium. A variety of silicon doping levels are offered, from 4 layers (2 p-type, 2 n-type) in the CEA-LETI platform to 7 layers (4 p-type, 3 n-type) in the OpSIS-IME platform. Germanium dopants to build p-i-n photodiodes are also offered. The CEA-LETI Heater platform is unique in offering a Ti/TiN heater module. After silicon etches, ion implantation and germanium growth, the metal stack is fabricated. The back-end includes patterning of the metal vias, contacts, interconnects and pads. The OpSIS-IME platform uses aluminum for the vias and for two levels of interconnects. Both the CEA-LETI platform and the IMEC platform use a single level of copper interconnects, AlCu pads and Tungsten vias. The OpSIS-IME platform cross sections is shown in Figure 2.
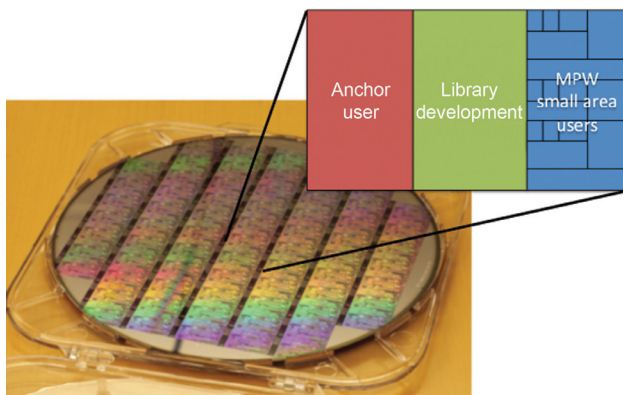

Figure 1   Photograph of an 8″ SOI wafer fabricated by the OpSIS-IME MPW service with an inset showing the how the die area is divided amongst users.

Table 1 Silicon height offered by different foundries. All foundries also offer a fully etched layer.

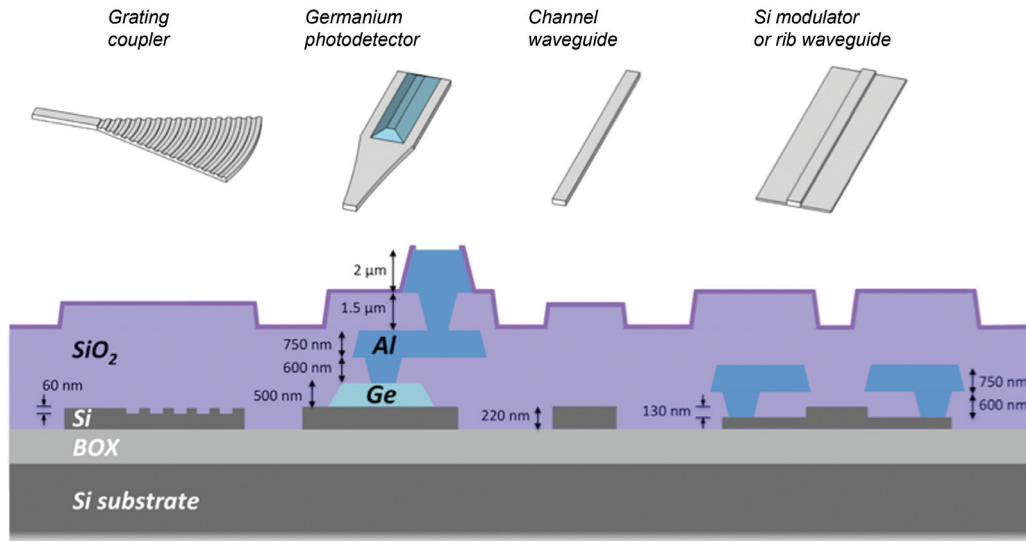| Silicon height (post etch)	OpSIS-IME	CEA-LETI	IMEC	IHP
Unetched silicon (nm)	220	220	220	220
Grating coupler layer (nm)	160	150	150	150
Slab layer (nm)	90	100	60	Not Offered

Figure 2   Cross-section of the OpSIS-IME platform.

3 Device library

Silicon photonic device libraries ideally contain a large number of passive and active devices as shown in Figure 3. Extensive testing must be conducted to characterize the cross-wafer and cross-lot performance of these devices. In this section, we will report primarily on the devices from the OpSIS-IME platform available in the PDK. The average and standard deviation measurements that follow are from cross-wafer testing.

4 Passives

Reliable and low-loss passive components are essential building blocks for larger photonic systems. Key passive
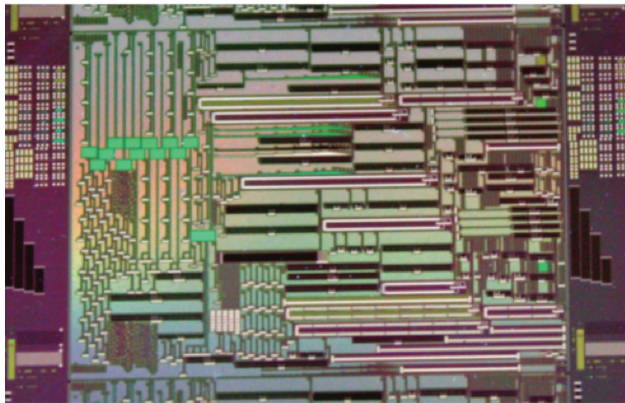

Figure 3   Photograph of an SOI photonic chip fabricated by OpSIS-IME showing a larger number of devices fabricated on a single die.

components include waveguides, grating couplers [13], distributed Bragg reflectors (DBRs) [14], waveguide crossings [15], and arrayed waveguide gratings (AWGs) [16].

4.1 Waveguides

Due to the high refractive index contrast between silicon and silicon dioxide, it is possible to design tightly confining submicron waveguides. However, larger waveguides have lower propagation loss. The standard single mode waveguide is a channel waveguide with a width of 500 nm and has a loss of 2.0±0.2 dB/cm in the OpSIS-IME platform. The standard routing waveguide consisting of a 1.2-µm wide rectangular channel was measured to have an average propagation loss of 0.36±0.10. Rib waveguides with 0.5 µm width and 90 nm slab thickness had an average loss of 1.7±0.5 dB/cm. Similar waveguide performance is reported from other silicon photonics platforms. The IHP passive platform reports a channel waveguide loss of 1.9 dB/cm and the IMEC full flow (http://www.euro-practice-ic.com/SiPhotonics_technology_imec_ISIPP25G.php) average loss is reported to be 2.3 dB/cm.

4.2 Grating couplers

Grating couplers are used extensively on the OpSIS-IME platform to couple light on and off chip, in particular because they enable efficient wafer-scale testing. The library TE grating coupler uses a single, shallow silicon etch of 60 nm (leaving a 160 nm thick silicon layer) and can
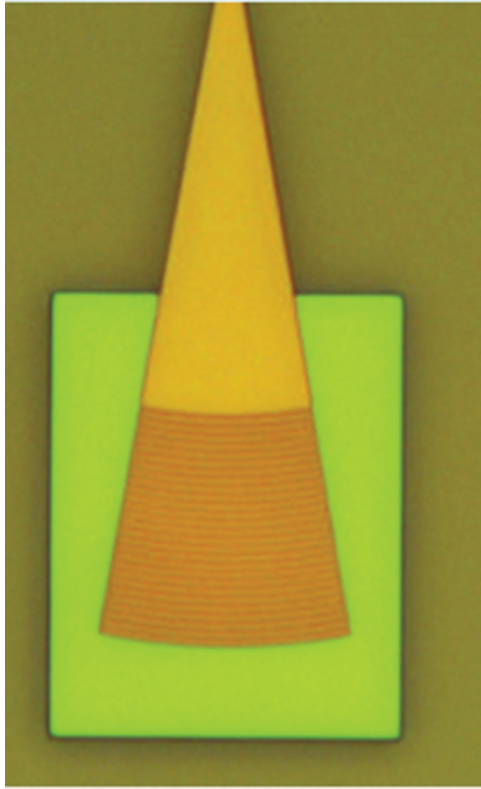
Figure 4 Optical image of a grating coupler. The box denotes the extent of the grating coupler (160 nm) silicon layer.

Figure 5 Simulated E-field distribution of a y-junction at 1550 nm.

be seen in Figure 4. Non-uniform gratings were designed to better match the diffracted profile with single mode optical fibers. Grating couplers on the OpSIS-IME platform achieve a cross-wafer average insertion loss of 3.1 dB at 1550 nm with a 1.5 dB bandwidth of 50 nm. The IMEC platform uses a poly-Silicon layer to achieve an improved loss of 2 dB while the IHP platform insertion loss is at 4.5 dB.

4.3 Y junctions

A consistent and low loss 50/50 splitter is often needed for photonic systems. To minimize insertion loss, the OpSIS-IME platform uses an optimized y-junction geometry that has been tested to have 0.28±0.02 dB insertion loss [17]. The simulated electric field can be seen in Figure 5.

4.4 Waveguides crossings

Another passive component available for system building is the waveguide crossing. Using similar simulation techniques as with the Y-junction, the insertion loss was optimized using finite-difference time-domain (FDTD)
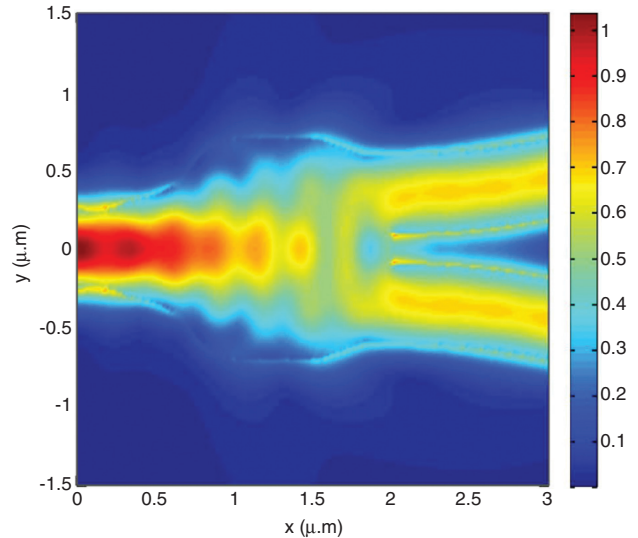
simulation. Cross wafer measurements showed an insertion loss of 0.18±0.03 dB with a cross talk of -41±2 dB [15].

5 Modulators

Silicon modulators commonly employ the plasma dispersion effect in which the refractive index is changed by varying the free carrier densities [18]. Modulators in the OpSIS-IME platform employ both the plasma dispersion effect and thermal tuning. Thermal modulators are relatively slow and are in use most often in low-speed application such as in switches and tuning [19].

5.1 Traveling wave modulator

Traveling wave Mach-Zehnder (TWMZ) interferometers have been demonstrated operating at speeds of up to 50 Gb/s [20, 21] with power consumption on the order of 200 fJ/b at 20 Gb/s [22] and a high linearity of 97 dB·Hz$^{2/3}$ [23]. The OpSIS-IME platform also employs these modulators using a 3 mm active length with a metal coplanar transmission line of 33 Ω impedance. The modulator uses a lateral p-n junction with six doping levels (p++, p+, p, n++, n+, n). The highest doping level enables low resistance via contacts, the medium doping enables lower parasitic resistance in the slab layer and the lowest doping is used to form the junction with minimal free carrier losses. The net insertion loss of the device, excluding routing and coupling, was measured to be 7 dB. By applying
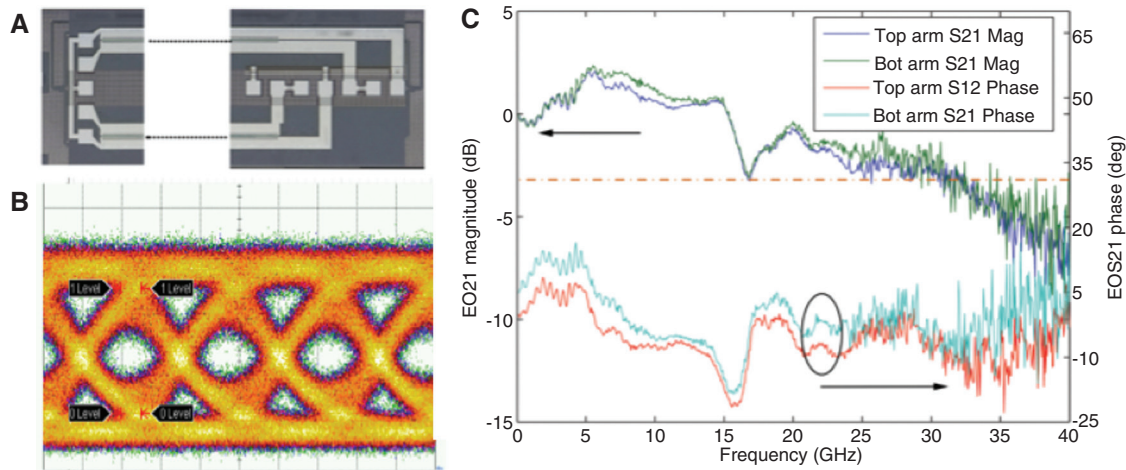
Figure 6 (A) Optical image of traveling wave modulator. (B) Eye-diagram at 40 Gb/s under differential-drive with 0.25 V bias and 2.5 Vpp drive voltage. (C) RF performance at 1 V bias. The amplitude shows a 3 dB bandwidth of 30 GHz.

a DC bias, the small signal Vπ was measured to be 7 V. The 3 dB bandwidths of both arms were measured to be over 30 GHz with <1 V bias. The eye diagram at 40 Gb/s with 0.25 V bias and 2.5 Vpp driving voltage is shown in Figure 6B. Under these conditions 5.1 dB extinction ratio was achieved with excess loss (due to modulator biasing) of 1.7 dB. Note that the drive voltage listed above is measured at the output of a 50 Ω instrument; actual voltages on the device are slightly lower (voltage intake is 67% for a 25 Ω termination at low frequencies). The IMEC platform lists 20 GHz performance for their TWMZs.

5.2 Ring modulator

Using the resonance of a structure such as a ring, both device footprint and power consumption can be significantly reduced, although at the expense of a narrow operating range and high sensitivity to thermal and fabrication variations. Ring modulators have been shown to work up to 40 Gb/s [24] with power consumption as low as 7 fJ/b at 25 Gb/s [25]. Ring modulators are also available in the OpSIS-IME platform. The rings are built with a 12 μm radius using 0.5 μm wide rib waveguides. The typical Q factor and free spectral range were measured to be 2800 and 7.65 nm, respectively. The small signal tunability was measured to be 28 pm/V (see Figure 7A) and the 3 dB bandwidth was measured by a VNA to be 45 GHz at 0 V bias (see Figure 7B). It is estimated that these rings will achieve 5 dB extinction ratio when driven by a 2.4 Vpp signal and when the '1' bit is biased to have 7 dB modulation loss. Ring modulators on the IMEC platform achieve a bandwidth of 20 GHz.
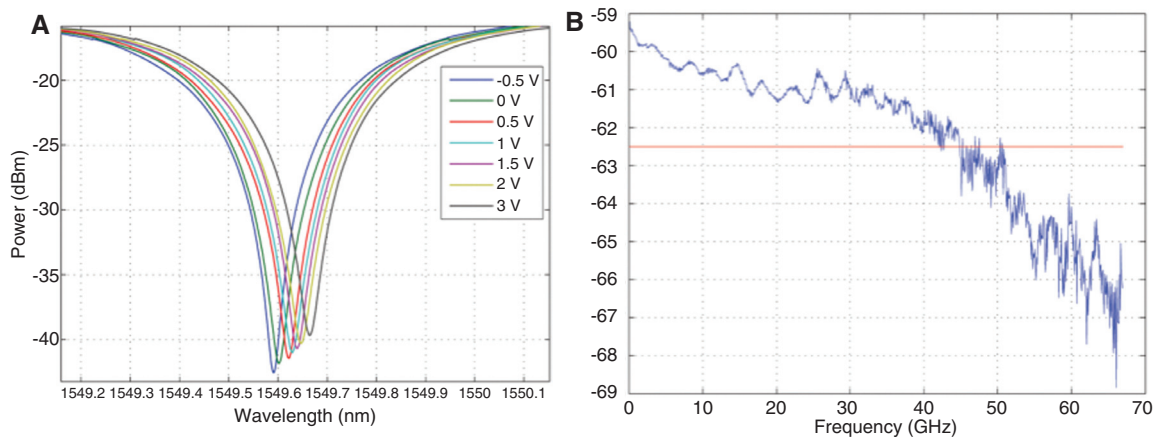

Figure 7 (A) Resonance wavelength at various bias voltages. (B) EO response at 0 V bias showing a 3 dB bandwidth near 45 GHz.
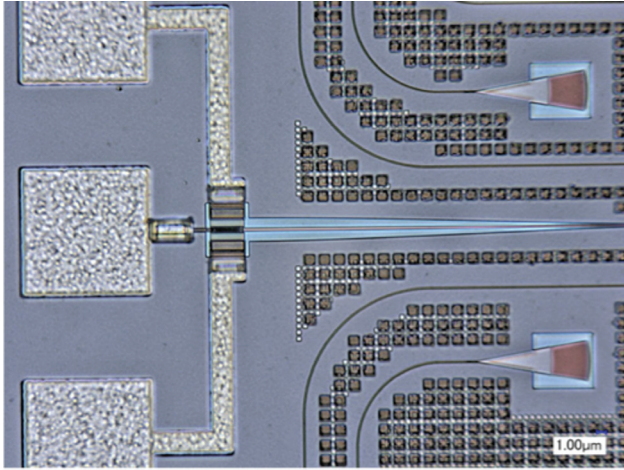
Figure 8 Micrograph of a basic Germanium photodetector without an inductor for gain-peaking (500× magnification).

6 Detectors

Germanium is commonly used as the detection medium due to its compatibility with the silicon material system. State of the art germanium photodetectors have shown bandwidths up to 120 GHz [26] and responsivity as high as 1.05 A/W [27], though not yet in an integrated platform with modulators. The OpSIS-IME platform photodetectors use evanescently coupled Germanium photodiodes with a vertical p-i-n junction as shown in Figure 8. The germanium is 8 μm wide and 11 μm long at the base and is 500 nm in height. Cross-wafer testing measured a responsivity of

0.74±0.13 A/W at 1550 nm and a dark current of 4.0±0.9 μA at 2 V reverse bias. The electro-optic (EO) response of the detector was enhanced by inserting a spiral inductor in series with the photodiode (see Figure 9A). This peaking technique increased the 3 dB bandwidth from about 20 GHz for the same unpeaked geometry to 58 GHz as seen in Figure 9B. The detectors on the IMEC platform have an unpeaked bandwidth of 50 GHz at -1 V bias as well as a responsivity of 0.5 A/W and a dark current of <50 nA.

7 PDK development

A number of components are under development for the next generation of the PDK. As more devices are added to the PDK and as the current devices continue to improve, the number of applications that can be serviced by this platform will multiply. A comparison of a selection of devices from different OpSIS-IME PDK versions can be seen in Table 2.

One capability that we hope to fully integrate into the OpSIS-IME platform is 1310 nm compatibility. Separate versions of all passive devices (grating couplers, y junctions etc.) that will work at 1310 nm are currently undergoing qualification. Active devices (modulators, detectors) will also be modified and characterized to work as a part of 1310 nm systems.

A second capability that will also be integrated into the OpSIS-IME PDK in the near term is polarization diversity,
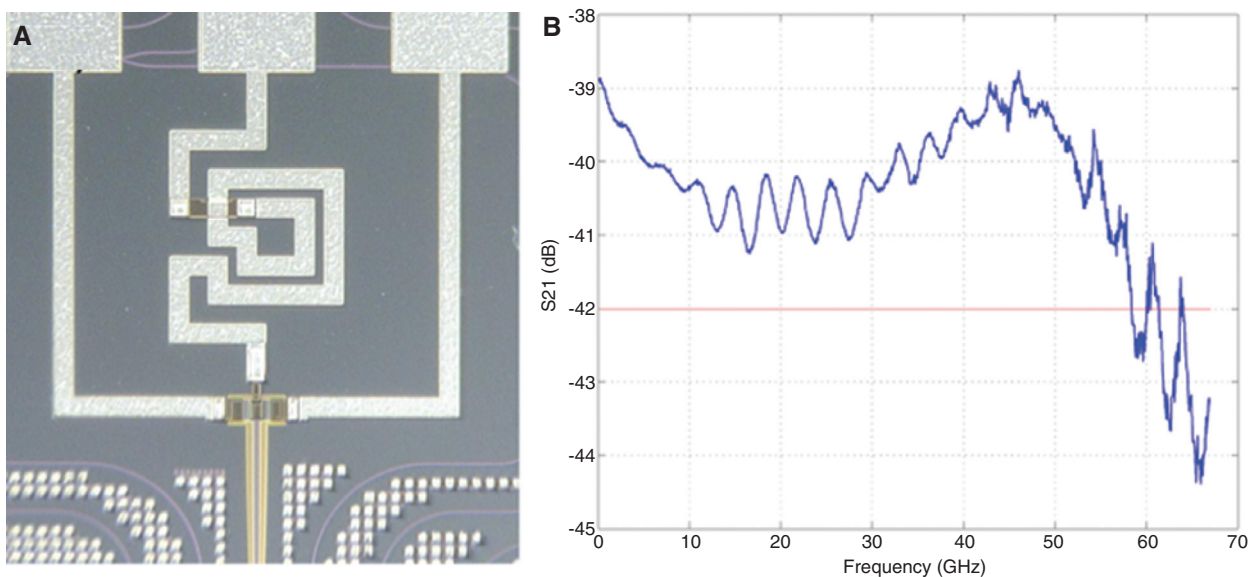

Figure 9 (A) Image of gain peaked photodetector showing the spiral inductor. (B) EO response of the peaked inductor with a 3 dB bandwidth of 58 GHz.

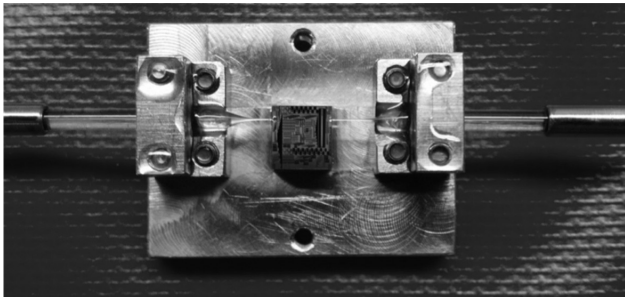**Table 2** OpSIS-IME PDK device performance data at different versions of the PDK.

	OpSIS-IME PDK V2	OpSIS-IME PDK V1
Modulators and detectors		
Ge PD (V2 uses gain peaked)	0.7 A/W, 58 GHz	0.54 A/W, 20 GHz
Ring modulator	28 pm/V, 45 GHz	11 pm/V, 19 GHz
Traveling wave MZ	7 V Vπ, 30 GHz	7 V Vπ, 15.8 GHz
Passive components		
Y-junction	0.3 dB IL	1.3 dB IL
WG crossing	0.18 dB IL	
Grating coupler (TE)	3.1 dB IL	3.7 dB IL
1.2 µm wide channel WG	0.4 dB/cm	
500 nm Rib WG	2.0 dB/cm	2.4 dB/cm

The devices that do not have performance data in PDK V1 are new devices in PDK V2. Note that small-signal Vπ values are listed for the TWMZ

or the ability to manipulate both TE and TM polarizations. Devices currently under development to support polarization diversity include TM grating couplers, polarization splitting grating couplers (PSGCs) and polarization rotators (to convert TM to TE mode). We expect to provide polarization diversity at 1550 nm as well as 1310 nm.

8 Packaging

Another service offered by the foundries is optical packaging for the silicon chips. OpSIS packaging options include vertically incident coupling through PLC Connections (http://www.plcconnections.com/) and edge coupling available with Chiral Photonics (http://www.chiralphotonics.com/). Figure 10 shows an example of how a chip can be packaged with edge couplers. PM fibers with tapered spot-size converters with 2 µm mode field diameter are used to couple light into the chip and an insertion loss of 2 dB per facet and polarization extinction

Figure 10 Photograph of a silicon chip in its optical package to polarization-maintaining fibers. Edge coupling to tapered silicon waveguide is achieved with a spot-size-converters in the fibers.
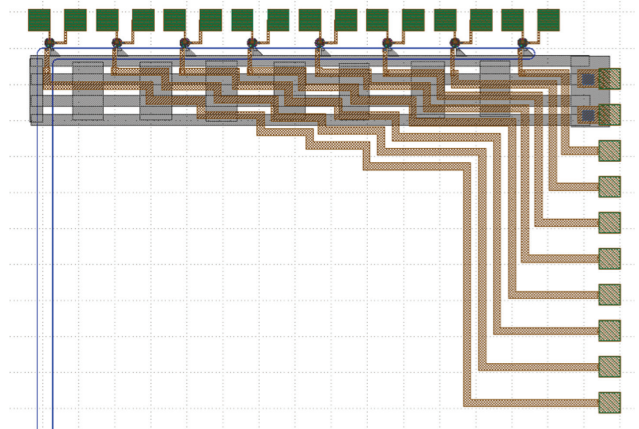
ratio >20 dB has been measured. The Chiral packaging option through OpSIS has been tested at cryogenic temperature with unchanged performance and demonstrates good robustness for a wide range of applications and environments. Similar edge and grating packaging solutions are offered by ePIXFab in collaboration with the Tyndall National Institute (http://epixfab.eu/images/documents/packaging%20announcement.pdf).

9 A transition from devices to systems

One noticeable development from the first few OpSIS-IME shuttle runs is that many users, when presented with a library of functioning devices, chose to focus on building systems rather than modifying devices. This signifies that the basic devices are good enough to move the focus from iterating on device geometries to building application-specific photonic integrated circuits (as-PICS). The ability to use such basic devices as building blocks and have a reasonable expectation of a system of operating in the first tapeout is a powerful capability for the fabless photonics community. For example, a validated thermally-tuned ring modulator cell can be used to build WDM system such as the one shown in Figure 11. We expect such a capability will spark rapid growth and innovation of complex photonic systems.

10 System design flow

As users begin to build larger, more complex photonic systems, it becomes even more imperative to have the

Figure 11 Layout of an 8-channel WDM ring transmitter with pads for RF driving (North) and for DC thermal tuning pads (East).

tools to simulate and optimize such systems. OpSIS is currently working with Mentor Graphics (http://www.mentor.com/) and Lumerical (http://www.lumerical.com/) to develop a set of tools for such a complete design flow. OpSIS users work in Mentor Graphics Pyxis® for schematic capture and layout, with integrated designed rule check (DRC) and layout versus schematic (LVS) tools by way of Calibre nmDRC™ and nmLVS™. From there, optical circuits may be exported to Lumerical Interconnect for systems simulation. While still in development, these tools are available to OpSIS users in order to take full advantage of the OpSIS-IME process design kit. A device library is also being developed in conjunction with Phoenix BV (http://www.phoenixbv.com/news.php?refID=3431).

Compared to the microelectronics industry, the compact models, schematics, and associated tools for photonic circuits are relatively immature. Tools such as Mentor Graphics Pyxis, Lumerical Interconnect, and the IPKISS component design framework are beginning to address the complex and unique needs of optical circuits. Nobody yet has a design flow that allows seamless movement between schematic design, layout, simulation, and electronics co-design. As the CAD infrastructure moves forward, it will be vital for near term adoption to standardize models and characterization techniques. Fortunately, industry organizations such as Si2 are now beginning to take on such issues.

Figure 12 Contour plot of cross wafer y-junction performance [17].

level of maturity and stability, but are not yet available to the wider community. Many structures in the current OpSIS PDK are geometrically simple, but it is still unclear how the variation, for example of waveguide loss, might affect a more complex device or system. While DRC is an important first step for yield, design for manufacturing rules will be necessary in the future for improving yield and reducing variance. A key area for near-term innovation is in developing devices whose key parameters are insensitive to fabrication variances.

11 Design for manufacturability and yield management

As users begin to take advantage of shuttle run services for developing commercial products, issues such as ensuring high yielding devices become critical. Within silicon photonics, there is significant area for improvement. The basic structures such as waveguides, grating couplers and directional couplers that are necessary for photonic systems are quite different from the critical structures of conventional electronic CMOS processes. Furthermore, there have been only limited efforts to understand how standard process techniques in the electronics world, such as optical proximity correction, affect the photonic devices.

The devices in the OpSIS PDK are tested for cross-wafer performance, with performance deviating by typically less than a dB per device as shown by the wafer scale y-junction loss in Figure 12. Yield and variation data between different lots continues to be generated as more silicon is run, and will be vital for continuing development. Commercial processes like Luxtera's are at a higher
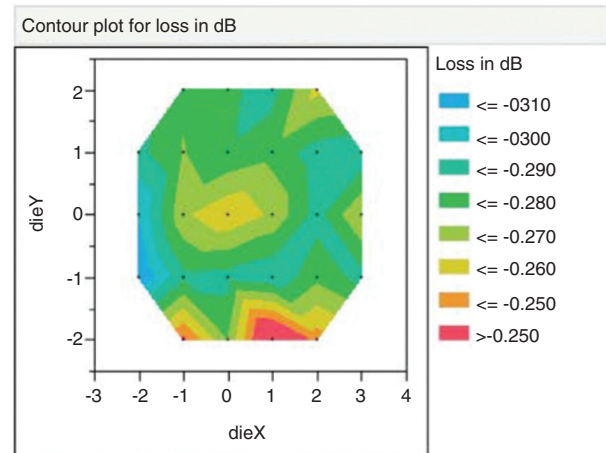
12 Electronic-photonic integration

The close integration of electronics with photonics can enable even more complex optical systems and boost the performance of photonic integrated circuits. For example, even low-speed electronic circuits could provide feedback to temperature stabilize devices, especially resonant components. While not yet offered through a foundry service, there are two primary categories of electronic integration: monolithic and multi-chip.

Monolithic integration can be achieved by either modifying existing CMOS processes to explicitly work with high-speed optics, or by building optical circuits within the constraints of an unmodified CMOS flow. Luxtera has achieved the former case with the Freescale 130 nm CMOS process [28], as has IBM with a 90 nm integrated CMOS process [29]. All of the electronics and photonics are fabricated in a single layer stack. This required significant development, and the addition of many layers in order to allow CMOS transistors, modulators, and germanium photodetectors to co-exist. On the other hand, unmodified CMOS or bipolar process integration is, on the surface,
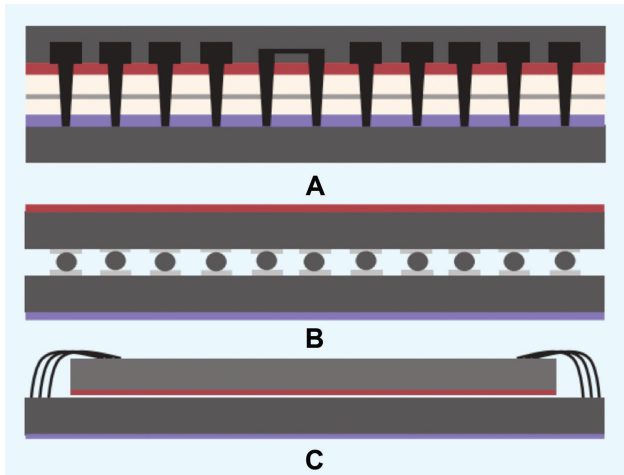
Figure 13 Electronic-photonic integration schemes: (A) Through-silicon vias, (B) Bump bonding, (C) Wire bonding.

attractive from a process development cost perspective [30]. However, a demonstration of high-speed devices has yet to be presented. Additionally, low-percentage silicon germanium restricts the allowed operating wavelengths for detectors to near the absorption edge in silicon.

OpSIS among other organizations is focused on multi-chip integration in which two chips are fabricated in separate processes and then bonded together. To some extent this is a product of necessity, given the high costs of developing monolithically integrated processes. But there are also significant advantages to this approach: First, both the electronic and photonic processes adapt over successive generations, which brings the benefits of best-in-class processes to both. Second, electronics processes benefit from much smaller critical dimensions than those needed by photonics. Fabricating the photonics separately allows a cheaper process to be used for the photonic devices, significantly decreasing fabrication costs. The disadvantage of the multi-chip integration approach is the need to make high-speed connections between the chips post-fabrication, and the associated logistical and supply-chain overhead. However, significant progress has been made in providing such high-speed connections. Electrical bonding techniques for multi-chip integration include wire bonding [31], flip-chip bump bonding [32], (which provides reduced parasitic capacitance and higher density than wire bonding) and through-silicon vias [33], which offer even higher density and lower parasitics (see

Figure 13). Copper pillar interconnects, at very low capacitance and high density, are already in production for electronics, and it is only a matter of time before they are used to attach high-performance CMOS and Bi-CMOS circuits to silicon photonic chips.

13 Conclusion

Rapid improvement in the available silicon platforms will likely continue in the near future. As the rate of device performance improvement slows and the processes mature, the focus will turn to the development of complex photonic systems. Unlike in electronics, photonic performance does not scale with linewidth, so progress will center for the next few years around the development of ever more efficient and complex systems, rather than on a Moore's Law like progression to ever smaller devices. Process standardization and device statistics will inevitably become more robust as additional silicon is fabricated. The importance of the development of design automation tools for building these systems cannot be emphasized enough. Photonic systems design tools are currently at the primitive stage of largely forcing users to do their wiring by hand. We can expect, over the next few years, the development of a much more diverse ecosystem of tool vendors, software providers, and an entire fabless semiconductor industry focused on silicon photonic design.

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