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Platform Specific FPGA Based Hybrid Active Power Filter for Power Quality Enhancement

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Abstract:
Elimination of harmonics by the use of power filters is required for power quality improvement; provides a wide area for the researchers to develop efficient power filters with improved control platforms. This paper motivates the implementation of the embedded control platform for better control of the power filters for faster elimination of harmonics. Although many embedded processors fascinates the implementation of the control techniques but finding the feasible platform is a great task. Software implementations are feasible for most of the power electronics converters but the hardware design with required digital hardware is a challenging task. The present paper deals with the development of the control technique for the Hybrid Active Power Filter with Xilinx System Generator Platform. The virtual FPGA (Field Programmable Gate Array) platform provided by the Xilinx System Generator has the ability to generate better switching signals for the control of the power filter to generate compensating signal for elimination of harmonics to maintain the power quality in the distribution lines. Experimental results obtained by the setup developed in the Power System Laboratory presents the effectiveness of the Embedded Platform. Various source voltage conditions also simulated and performance is verified for the developed Hybrid Active Power Filter.

Keywords: embedded system, harmonic elimination, hybrid active power filter, power quality improvement, Xilinx system generator

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1 Introduction

The Power Electronic devices are the major source for significant harmonic current which causes rise of different types of power quality issues in the power system. Maintaining the power quality in the distribution lines becomes necessary for elimination of the harmonic current. Passive Power Filters as well as Active Power Filters have been used to eliminate the harmonic current in the distribution network. Advancement in the power conditioning devices have been raised gradually considering the various power quality issues. Various type of passive power filter has been used in literature as LC type, LCL type, RL type. Passive filters can be classified into tuned filters and high pass filters. Installation of such passive filters are mainly to absorb high contain of harmonic current from flowing out in the circuit [1]. However due to the high volume and fixed compensation active power filters are introduced. Active filters are categorised in to single phase and three phase active power filters. Shut type APF and series type APF also developed [2]. However these devices has high resonance, fixed compensation, and cost becomes high for larger systems; require high power converter ratings. These drawbacks of Passive as well as Active power filter do not allow for further improvement down the line and forces the researchers to overcome these problems[1, 2]. Hybrid Active Power filters effectively overcome the problem related to passive as well as Active Power Filters and converge the advantages of both to provide a better cost effective solution for this power quality issue [3]. Hybrid active power filter can be shunt hybrid active filter which is considered for better current harmonics compensation and other type of hybrid active power filter like hybrid series active power filter used in series active power filter for voltage quality issues. Hybrid Active Power filters has one shunt Active Power Filter and one passive filter connected in parallel to the distribution line [4]. On the contrary to choose appropriate power filters, a perfect control algorithm is required to be implemented for the generation of switching signals. There are many control techniques proposed for the control of Hybrid Active Power filters such as synchronous detection technique, indirect control algorithm, P-Q method, space vector method.

Selected control strategy is required to be implemented with digital controller such as DSP or FPGA. *Shahram Karimi, Phillipe Poure* has reported [5] the implementation of control strategy on FPGA instead of DSP processors. *Bo Sun, V-Fat Chio*, demonstrated in [6], use of traditional approach FPGA processor for the development

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of the control law to generate the switching signal. However the embedded platform has several approach for the implementation of the control law on real-time hardware. DSP, FPGA and Microcontroller are the three basic categories of embedded platform. As many of the researchers have chosen FPGA for the design platform in spite of DSP and Microcontroller due to the faster processing capability [6, 7]. Development of the digital controller based on FPGA enhances the capability of the embedded control platform.

Section 4This paper motivates the researchers to develop the required digital controller based on embedded system design concept. It shows a new efficient, faster and cost effective approach for the implementation of the controller based on virtual FPGA or Xilinx System generator platform [7–11]. Harmonic elimination by the Hybrid Active Power Filter [12–15] requires efficient control schemes as well as faster development of the control schemes. Present paper demonstrates the implementation of the indirect control algorithm on Xilinx system generator platform which provide verification, testing and validation of the control strategy before downloading the code to actual hardware. Virtual environment of the system generator has the capability to develop automatic HDL code by choosing the required FPGA board [16, 17]. Automatic HDL code testing is done for the discussed problem of harmonic elimination. Comparison of the manual HDL coding and automatic HDL code generation is shown with its several aspects presented and discussed. Hybrid Active Power filter model developed in MATLAB/Simulink environment and the results shown in Section 4 with the Total Harmonic Reduction.

2 Configuration and control aspects

2.1 Hybrid acitve power filter

Figure 1 shows the detail configuration of the HAPF connected in parallel to the distribution system in between the source and nonlinear load. The connected diode bridge to the source is considered as a nonlinear load as it injects harmonics to the current in the distribution lines. HAPF has two parts includes one shunt APF containing IGBTs and passive power filter. The gate terminal of the IGBTs are switched by providing switching signals generated by the used Indirect Control Algorithm which is implemented on FPGA by Xilinx System generator development platform.

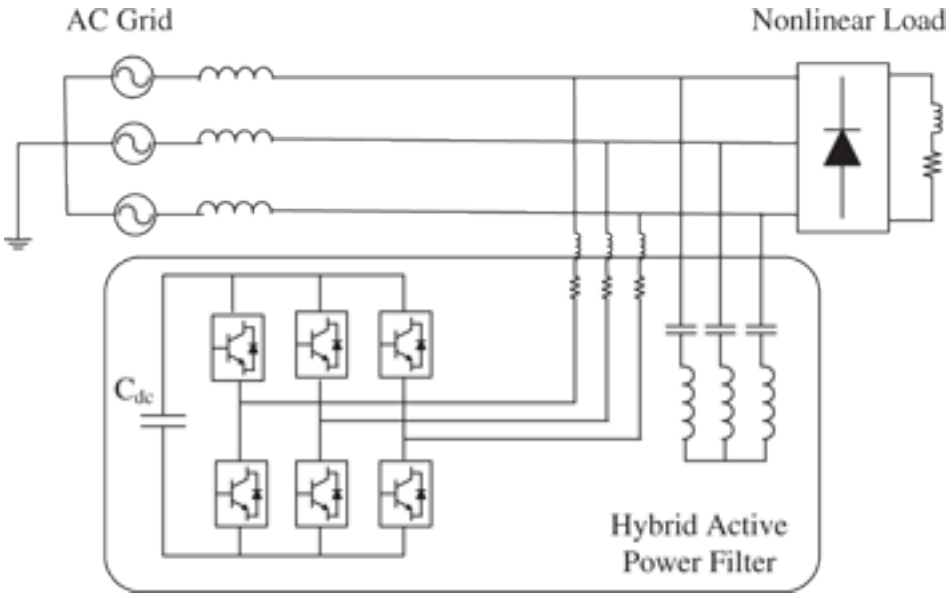

Figure 1: Configuration of the hybrid active power filter.

2.2 Control strategy

The voltage provided by the source can be represented as

$$v_s = V_m \sin wt \tag{1}$$

The current drawn by the nonlinear load can be represented as

$$i_L = \text{Load Current} = I_{m1}\sin(wt+\varphi_1)(\text{fundamental component}) + \sum_{h=2}^{\infty} I_{mh}\sin(hwt+\varphi_h)(\text{harmonics}) \quad (2)$$

The load current contains the active part of the fundamental current as well as reactive current with harmonic rich part added by the nonlinear loads. The Total Harmonic Distortion constitutes the harmonics as well as the reactive part which is required to be removed. The higher order terms represented in (2) can be eliminated by the low pass filter.

On the other hand multiplying $\sin\omega t$ both side of eq.(2), we get

$$i_L.\sin\omega t = \frac{I_{m1}}{2}\cos\varphi_1 - \frac{I_{m1}}{2}\cos 2\omega t\cos\varphi_1 + \frac{I_{m1}}{2}\sin 2\omega t.\sin\varphi_1 \quad (3)$$

At the present stage this current is required to be passed through LPF.

The current generated from the reference signal out of the filtered component can be obtained by multiplying with "2" which gives the result $I_{m1}\cos\varphi_1$. the capacitor voltage V_{dc} is compared with a reference value then it results an error, which is fed to a PI controller. To find out the peak value of the resultant current I_C which is added to the active reference current. Now the fundamental active reference signal can be generated by again multiplying $\sin wt$.

$$= (I_c + I_{m1}\cos\varphi_1)\sin\omega t \quad (4)$$

Subsequently following the same procedure the three phase indirect control algorithm is developed and the required block diagram for representation and easy understanding is show in Figure 2.

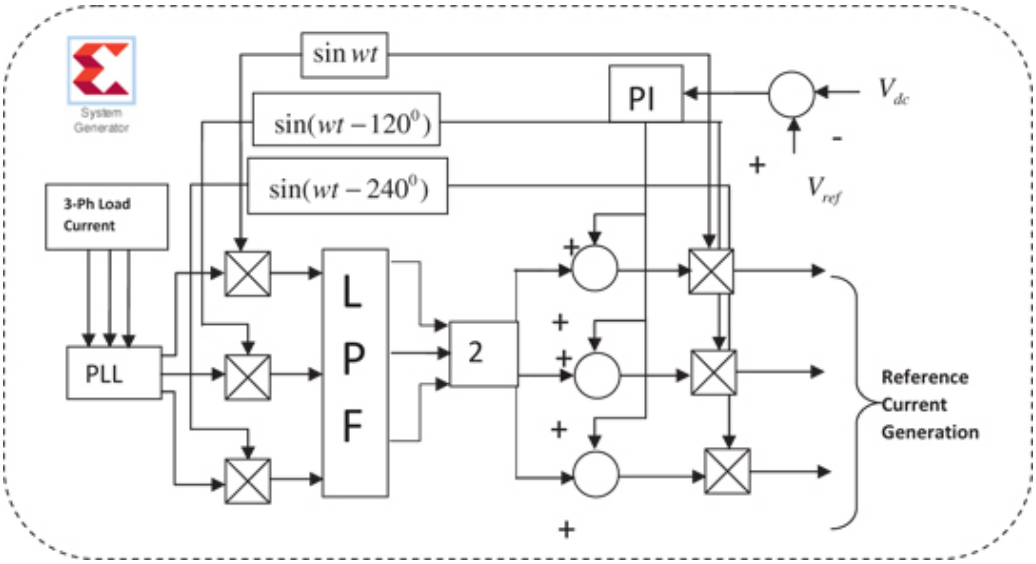

Figure 2: Block diagram of indirect control algorithm.

3 Platform specific controller development

System generator tool box is provided by Xilinx to link the Model Based MATLAB/Simulink design environments to develop FPGA designs. It provides a virtual environment for FPGA designs; Xilinx block set present in the Simulink library browser provides all the required design tools present inside an FPGA. The traditional FPGA design methodology of RTL (**Resistor transistor logic)**, Text bench generation is not at all required to develop or the hand written HDL code. All those process is taken care by the Xilinx system generator tool. Using the Xilinx block set is as simple as to use the Simulink environment blocks from the Simulink library browser. Thus System generator can be used for hardware modelling on an FPGA. The Xilinx block set contains adders, multipliers, delay, registers, get way in, get way out, Filters, FFTs etc. System generator uses the Xilinx ISE preinstalled and linked to MATLAB during initial stages. It has the special ability to generate automatically the

HDL code for the designed model. It automatically goes through the FPGA implementation steps to generate the bit file which is required to download to FPGA kit.

Previously the manual HDL coding is applied for the development of hardware configuration by VHDL code on an FPGA for which the design engineer has to spent time to learn coding techniques. The process of learning coding techniques consume time to a great extent. Although embedded design engineers has the importance to learn the coding techniques but at the present age scenario where time is big factor for every case, this embedded platform provides a time saving and efficient design technique. Figure 4 shows the comparison of system generator FPGA design and Manual method of FPGA design on timing constraints. This analysis considered six important features of the total FPGA design process; it can be clearly visualize that every design aspect of System Generator design platform consumes less time in percentage of total design time, comparison to the Manual FPGA design. Under various categories like functional design, HDL design, Hardware design, HDL verification has been considered for comparison analysis. Each category plays important role for the specific platform chosen. The data provided here are purely experimental which is obtained during the development of the control technique for hybrid active power filter and also tested for other cases. Figure 3 presents download of generated system controller code to FPGA board.

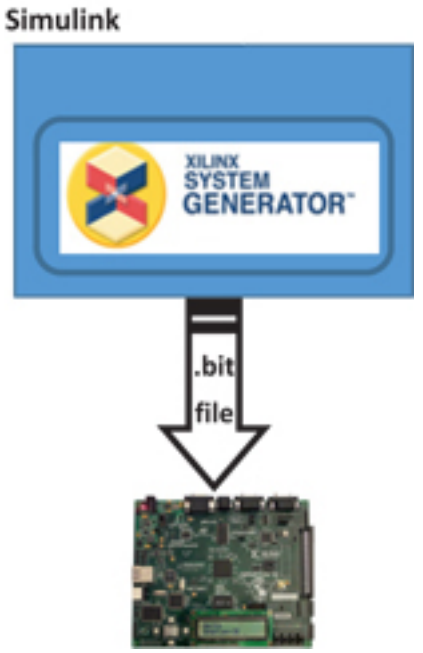

Figure 3: HDL code download to FPGA board.

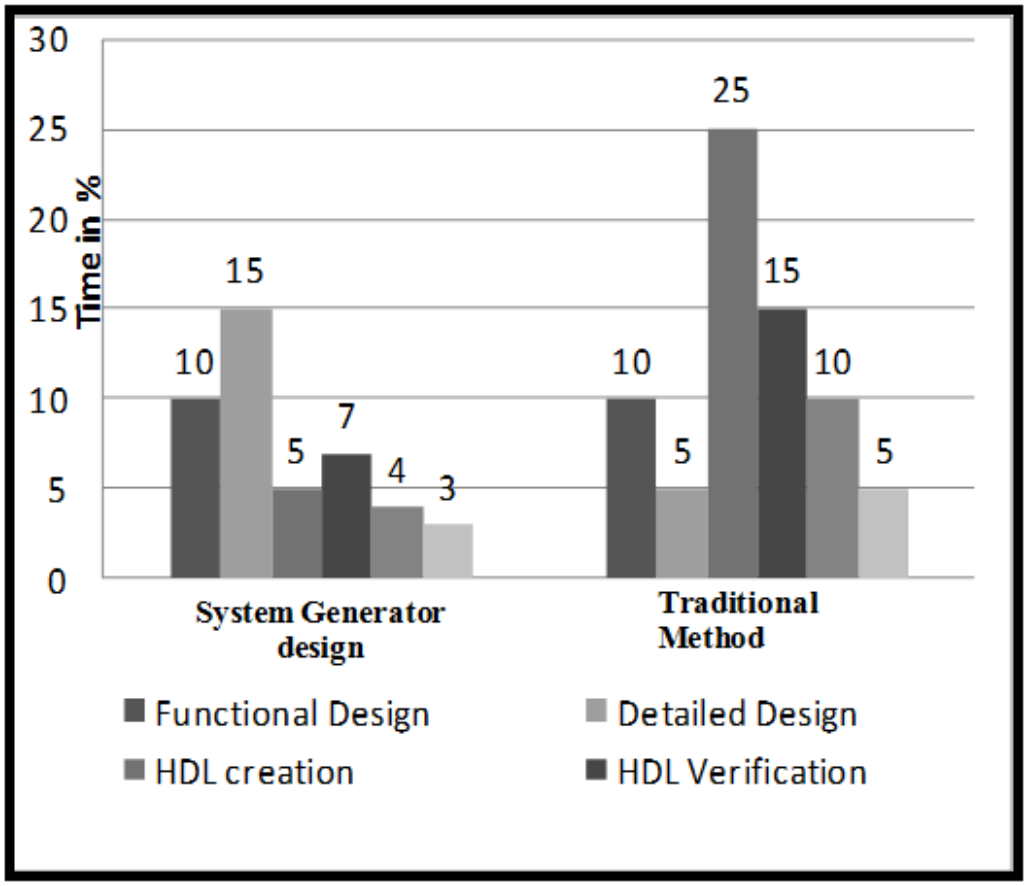

Figure 4: System generator vs. traditional HDL coding.

4 System generator modelling, results and discussion

Modelling of the indirect control algorithm in the System Generator platform requires the integration of the blocks of Xilinx block set such as adder, delay, register, constant, and multiplier into the simulink. The system Generator token is placed in the model for simulation to execute. The plant model of HAPF developed in the simulink environment can acquire the switching gate pulse for IGBTs from the System Generator control model by receiving the required voltage and current signals from the plant model. The system generator platform executes the controller part as virtual FPGA environment and generates switching signal to regulate the IGBTs. The proper compensation of the harmonics from the load current can be clearly visible in the results. Table 1 represents the parameters selected for simulation and the software details for developing the Xilinx system generator environment.

Table 1: System parameters.

Parameters	Specification
System voltage and frequency	230 V, 50 Hz
Source impedance	L_S: 2.5 mH, R_S: 0.3 Ω
Load AC impedance RL	5 kW
DC reference voltage	670 v
DC capacitor	2,200 µf
Switching frequency	10 kHz
FPGA, Software	SPARTAN3E Development Board, Xilinx ISE 14.2

[1] Table 1 with detail experimental specifications are concidered for hardware experimentation process.

4.1 Elemination of harmonic with 50 Hz source and balanced load

Feeding a balanced load by a 50 Hz, 230 V source is considered to be common which is found generally in consumer end. But the balanced load can be a nonlinear load able to inject harmonics to the power system. HAPF connected in shunt to the distribution lines compensate the harmonic signal. The proper compensation of the harmonics from the load current can be clearly visible in the simulated results. The required source voltage is shown in Figure 5(a) and the current drawn by the nonlinear load is shown in Figure 5(b). HAPF provides proper compensating signal reflected in Figure 5(c) for the elimination of harmonics in the distorted current and the current after elimination of the harmonics is shown in Figure 5(d). The THD obtained after compensation of the harmonics by the injection of compensating signal is shown in Figure 6. The figure clearly reflects the performance of the HAPF where the THD reduced to 1.6 % which is within the acceptable limit provided by IEEE 519 standard.

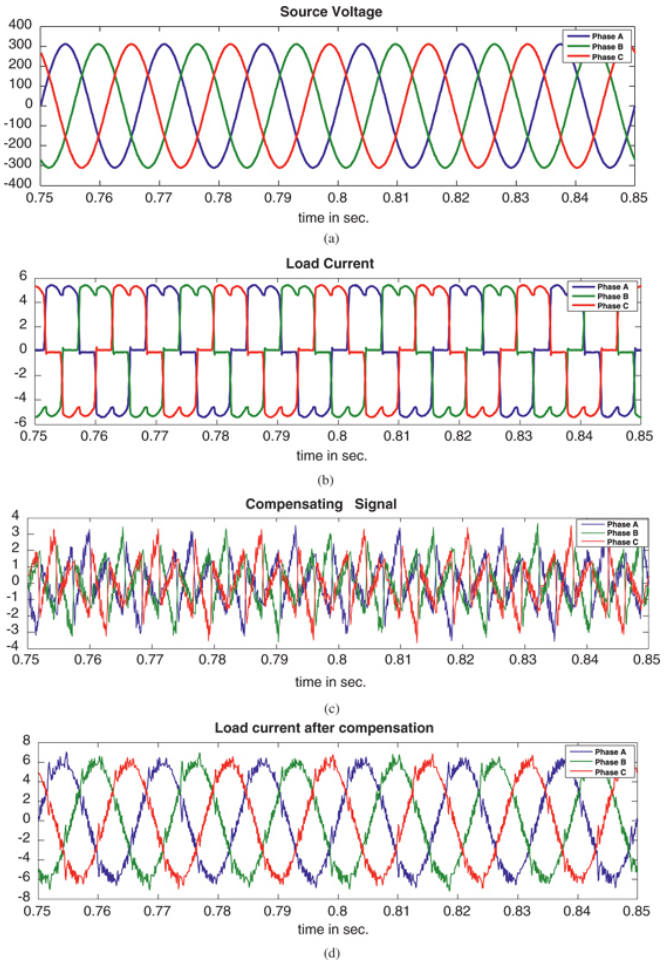

Figure 5: Simulation results obtained for ideal source and balanced load.(a) source voltage,(b) load current before compensation,(c) compensating signal, (d) current after compensation.

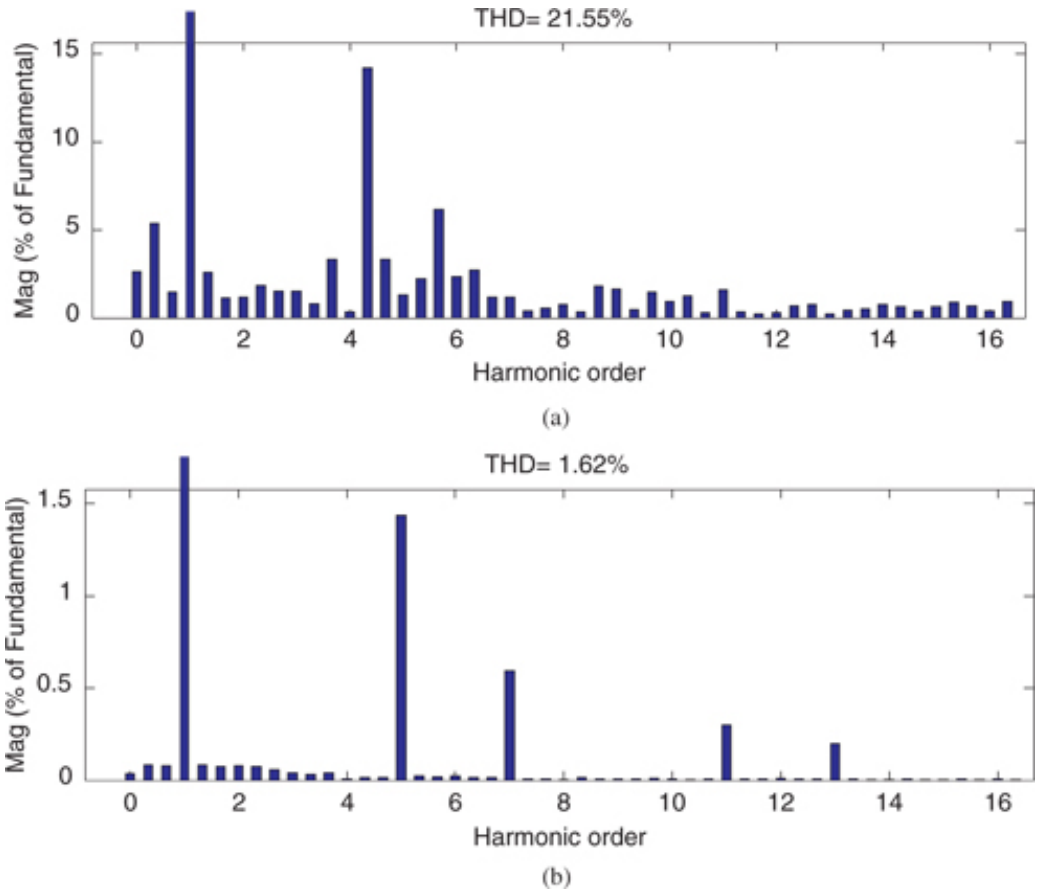

Figure 6: Total harmonic distortion for Ideal source voltage case (a) before compensation, (b) after compensation.

4.2 Harmonic elemination when distorted source feeding a balanced load

A sudden change in magnitude of voltage signal due to any arbitrary reason can affect the harmonic content in the power system. The magnitude of the voltage signal was suddenly raised by 10–20 % at approximately 15–30 s and fed to the same balanced load. The change in behaviour of the waveforms affects the performance of the control method implemented is shown in Figure 7. Although presence of distorted source the control method able to eliminate the harmonic content of the system considerably. Performance can be analysed by verifying the THD results as shown in Figure 8 which is reduced to 3.05 % after harmonic elimination.

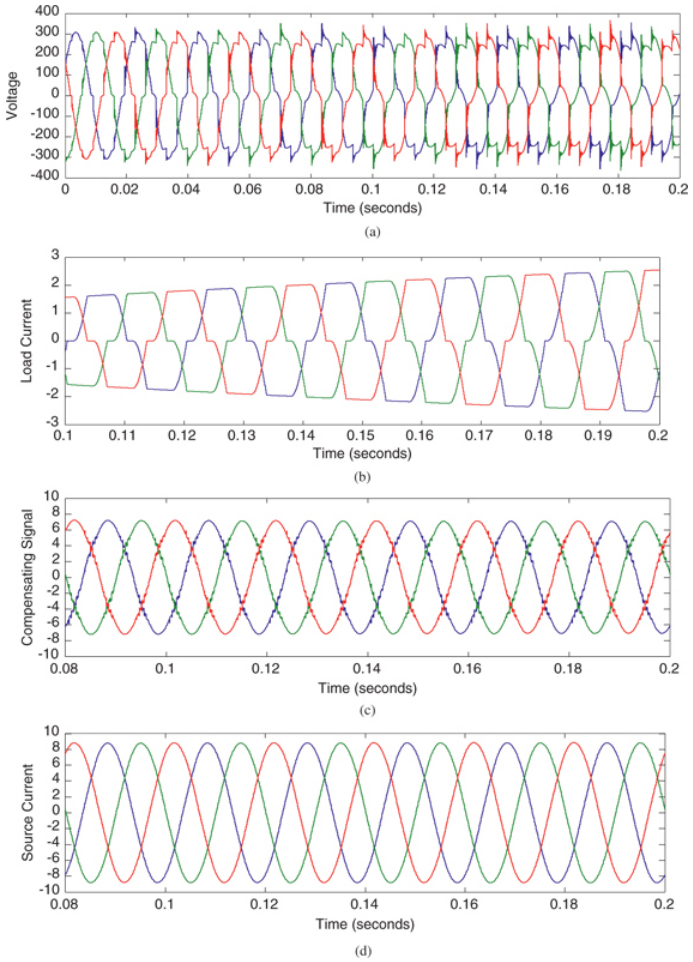

Figure 7: Simulation results for distorted source with balanced load : (a) source voltage, (b) load current before compensation, (c) compensating signal, (d) current after compensation.

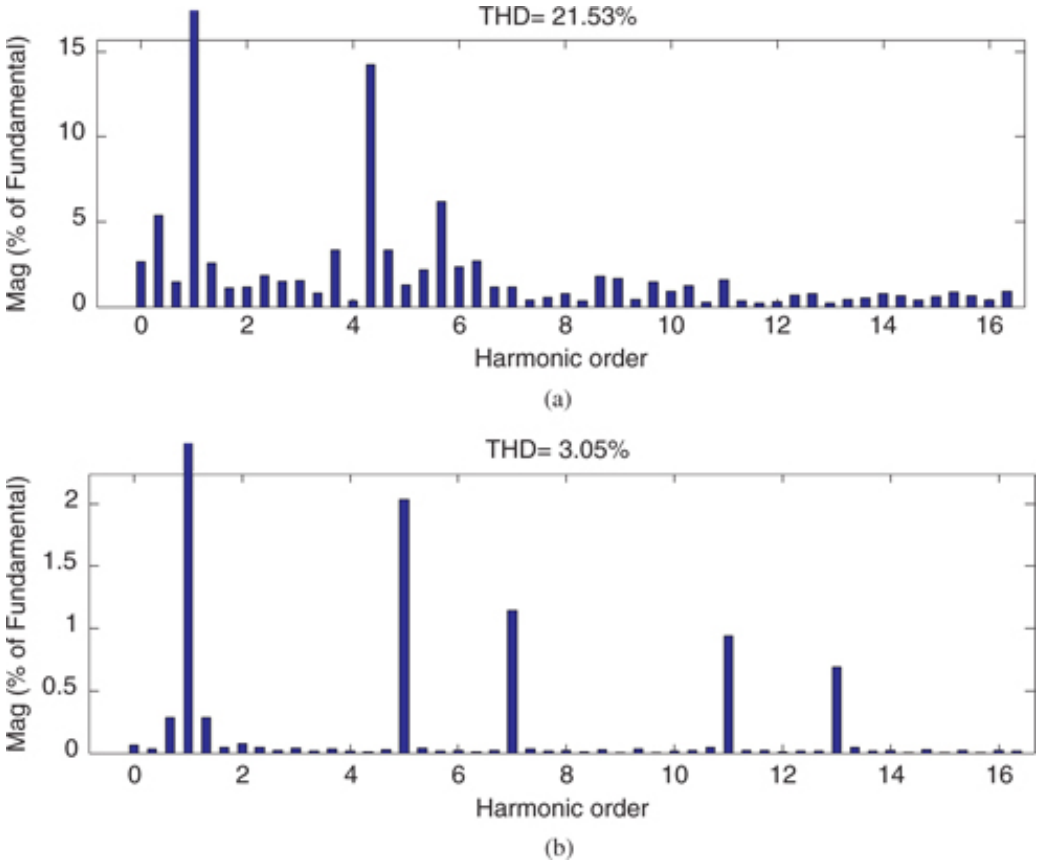

Figure 8: Total harmonic distortion for distorted source case (a) THD of load current before compensation, (b) source current after compensation.

4.3 Harmonic elemination when unbalanced source voltage feeding an balanced load

Present concept is validated through the simulation studies with the proposed HAPF configuration and ideal control strategies. The unbalanced source voltages with respect to the magnitude and the phase angle is shown in Figure 10(a). It is clearly visible from Figure 10(b) that the Load Current waveform are Nonlinear and unbalanced due to the Nonlinear Load R-L and unbalanced source voltage. The control scheme discussed is used for the harmonic compensation which results with the compensated source currents as shown in Figure 10(d). Total harmonic distortion of the load current and the source current after compensation is represented in Figure 10.

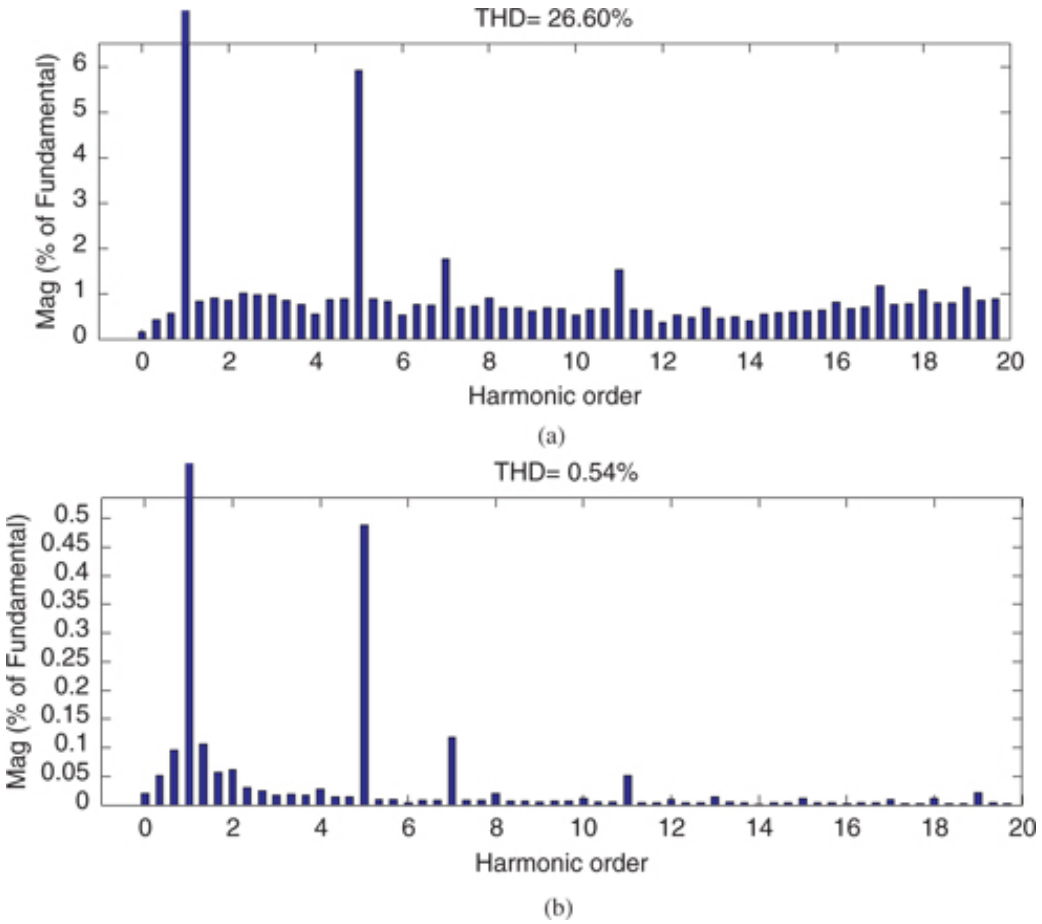

Figure 9: Total harmonic distortion for unbalanced source voltage case (a) Load current before compensation, (b) Source current after compensation.

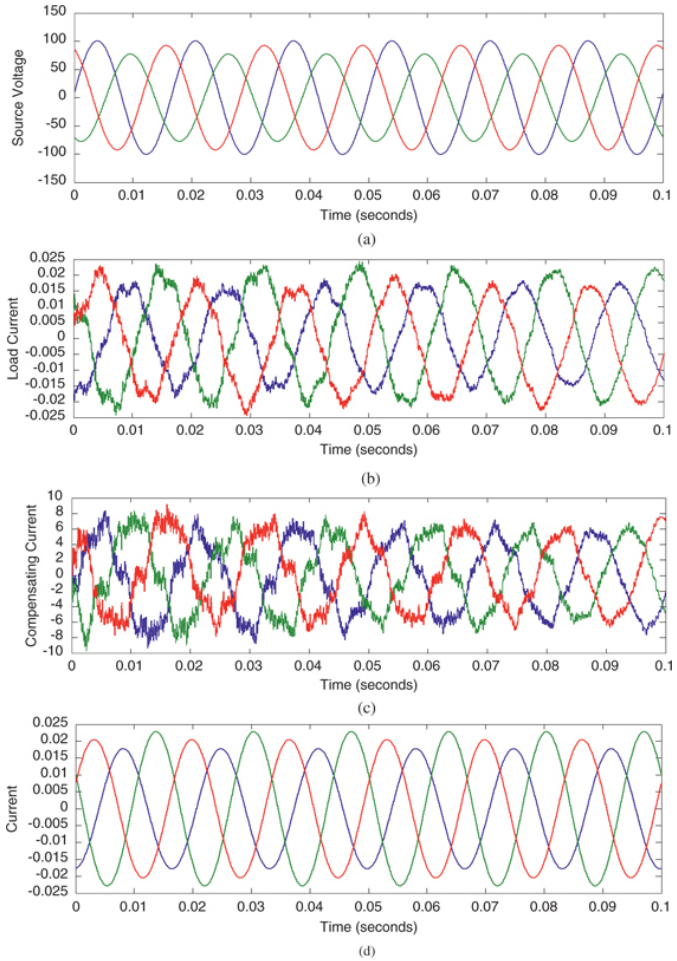

Figure 10: Simulation results for unbalanced source voltage case: (a) source voltage, (b) load current before compensation, (c) compensating signal, (d) source current after compensation.

5 Experimental studies and result

So far performance of the proposed control technique has been studied and simulated for different signals. It would be interesting to have the same on some experimental data that captures many more features arises due to the introduction of measurement and instrumentation errors. This section presents such studies. Pure balanced case is considered for the experimental verification. 230 V, 50 Hz source was act as input and voltage was supplied to the diode rectifier R-L load using an Isolation transformer. Rectifier makes the load non-linear and is the source of harmonics because of switching action of diodes. Figure 11 shows the detail configuration of the laboratory prototype developed.

Collected Voltage waveform taken at the terminals of isolation transformer captured in PC using a PC-PC communication Software. Source Voltage signals are sensed as shown in Figure 12(a). Algorithm is processed and the automatic generated bit file from the Xilinx System generator Environment is downloaded to the SPARTAN 3E development board. FPGA board specification is given in Table 2. Generated VHDL code is optimised for as per the available resources and constraints in FPGA which makes it suitable for actual hardware testing. Developed algorithm is required to download on the actual FPGA kit which will make it run with real plant signals. Nonlinear Load current for balanced case is sensed as shown in Figure 12(b). Experimental results obtained from unbalanced case is shown in Figure 13. Figure 13(a) illustrates the unbalanced source voltage, Figure 13(b) shows the unbalanced load current and the compensated current is shown in Figure 13(c). FPGA will receive the sensor output signals through which it is processed to generate the reference current and the necessary gate pulses. The switching signal generated by the FPGA is fed to the IGBTs of the HAPF to generate the compensating signal which is represented in Figure 14(a) and the experimental setup and Figure 14(b) shows the sensor board used for experiments.

Table 2: FPGA specification.

Technical specification of FPGA	
Device	XC3S500E
Input/output channels	232
Available differential i/o pairs	92
Compatibility	3.3 V
I/O package	fg320
System RAM	360 K
Clock	33 MHz

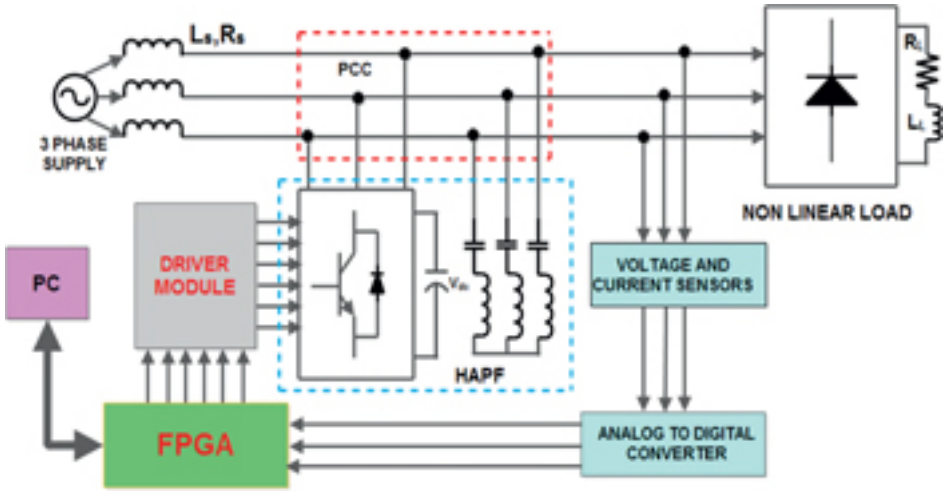

Figure 11: Block diagram of experimental set up.

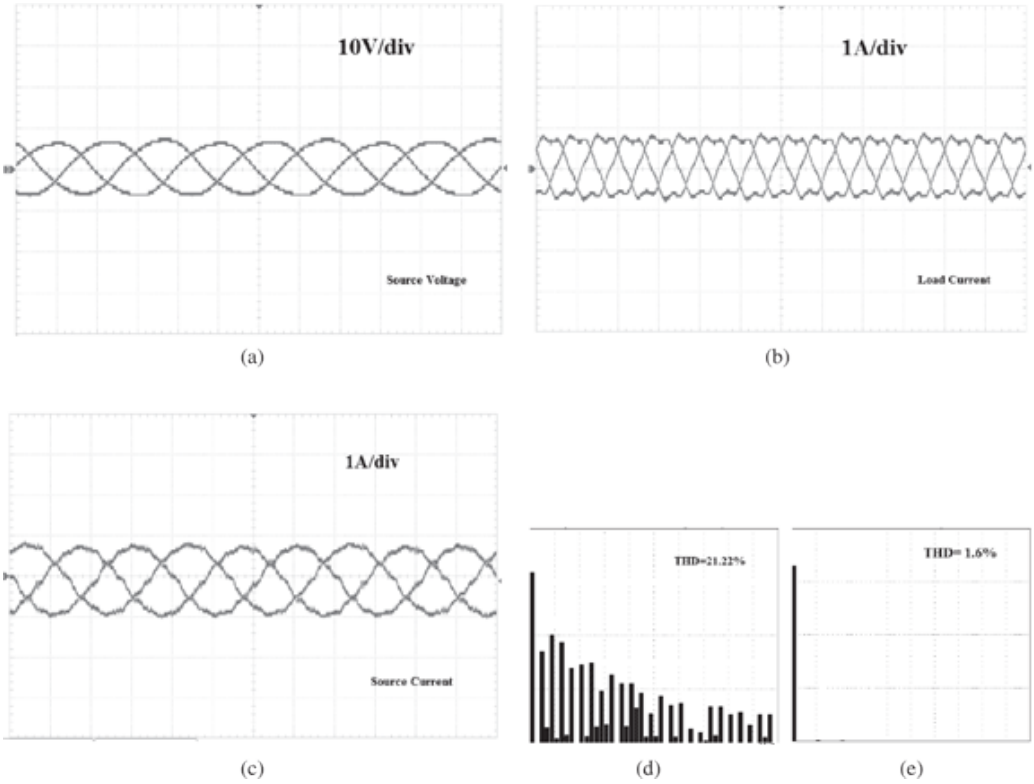

Figure 12: Experimental results: balanced case (a) source voltage, (b) nonlinear load current, (c) source current after compensation, (d) total harmonic distortion before compensation, (e) total harmonic distortion after compensation.

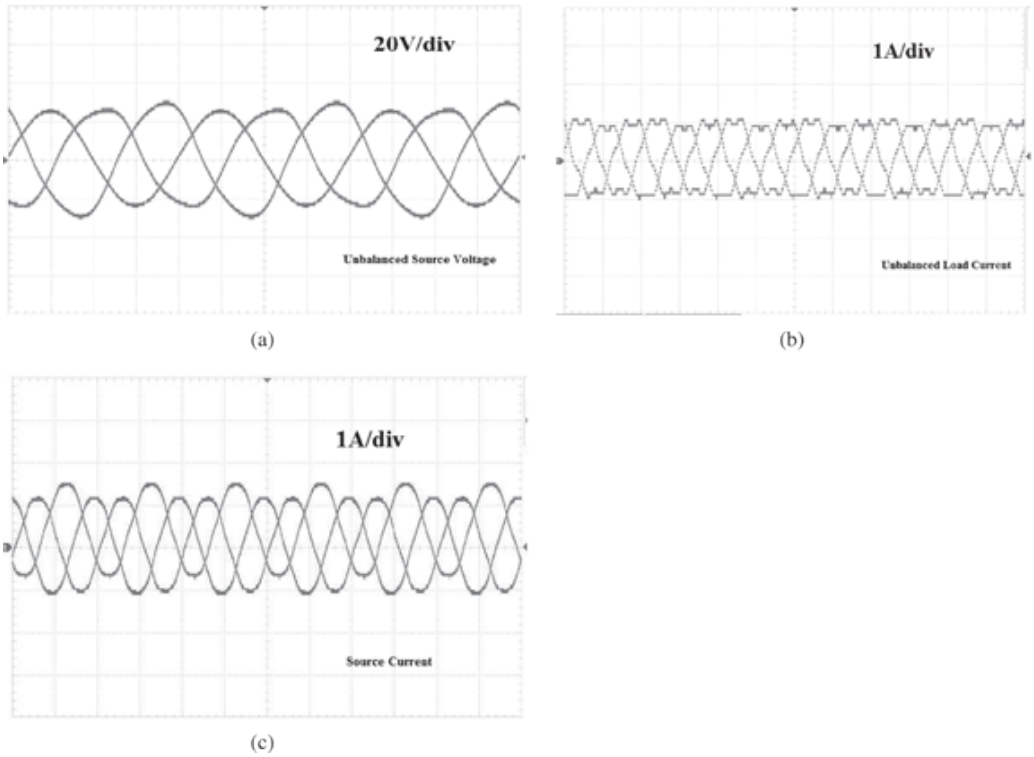

Figure 13: Experimental results: unbalanced case (a) source voltage, (b) nonlinear load current, (c) source current after compensation without harmonics.

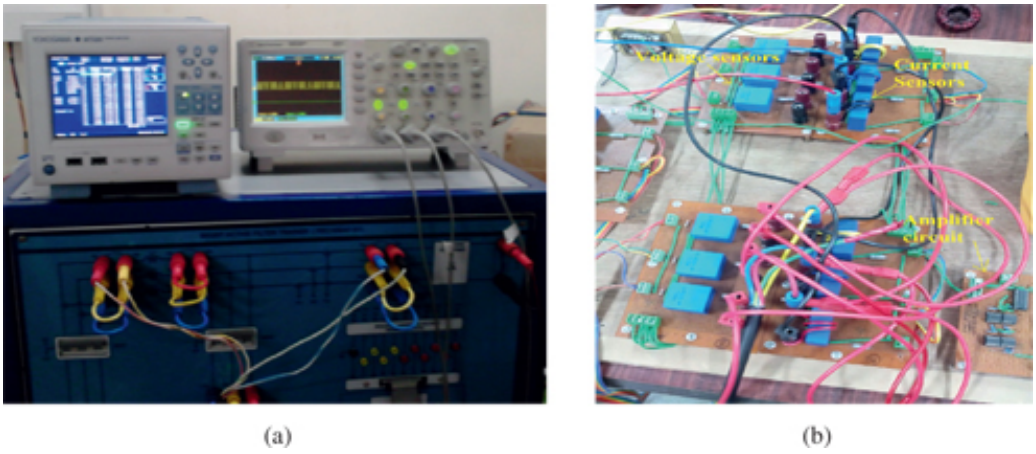

Figure 14: (a) Experimental set up with FPGA switching signal generation, (b) sensor board.

6 Conclusion

In this paper, it is presented that the faster method of controller design by system generator embedded platform is simulated, tested and verified. The mentioned method accelerates the indirect controller design for HAPF switching by providing virtual FPGA environment and made possible for testing, verification and validation of the model. Indirect control algorithm implemented with HAPF caused to reduce the harmonics from 21.59 % to 1.6 % and current waveform to be approximately sinusoidal. According to the justified range of reduction of the harmonics by the HAPF with time saving features compared to Manual HDL coding, system generator embedded platform has been verified successfully, results investigated and its effectiveness has been confirmed. The present embedded platform is also simulated and tested for unbalanced and distorted source condition where it provides excellent performance of the compensator to maintain sinusoidal source current.

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