Research Article

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Designing of a dual-functional XOR block in QCA technology

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Abstract: Quantum-dot cellular automata (QCA) technology was proposed as a way to implement digital circuits with a transistorless approach for overcoming CMOS limitations in terms of short channel effects and scale-down continuity. The main building block in QCA technology is the square cell with a couple of free movement electrons, the electrons' configuration inside the cell gives the cell the ability to represent binary information. Researchers were attracted to QCA because of its impressive features such as size and speed. Many important circuits, such as multiplexers and exclusive-OR, were presented in QCA technology with various layouts, looking for reducing the main metrics such as cell count, area, and implementation cost. In this work, a dual functional XOR block is proposed. The proposed block can function as a 2-input XOR or a 3-input XOR, providing greater flexibility. When compared to earlier 3-input XOR gates that did not have the dual function, the results show a significant improvement in cell count, area, and cost of about 7%, 50%, and 54%, respectively. The QCADesigner software is used to design the block as well as for verification issues.

Keywords: QCA technology, QCA-XOR, QCADesigner, nanotechnology, nanocircuits

1 Introduction

Many nanoscale technologies, including CNFET, FinFET, and Quantum-dot Cellular Automata (QCA), have been developed as a result of the growing market needs for electronic circuits during the past few decades in terms of size, fast speed, and efficiency. The transistors' small size and introduction into the nanoscale caused a number of issues with leakage current and energy consumption brought on by quantum phenomena. According to the International Technology Roadmap for Semiconductors study, QCA technology offers a novel approach to computation that represents a glimmer of hope of achieving nano-computers that operate at THz-level rates. The general purpose gates such as multiplexer [1–5] and XOR [6–12] have attracted many researchers due to their ability to reduce the complexity of the circuit. Therefore, the improvement of these gates is beneficial to the circuits that use them, thus reducing the cost. In this work, a new structure of the XOR block is proposed in QCA form. The proposed architecture has two functions where it can represent 2-input XOR or 3-input XOR. This option gives the block flexibility to be utilized in different circuits.

2 QCA background

The QCA technology is based on the principle of electrons' repulsion, as the basic building block is a small cell with a shape as shown in Figure 1. Logic gates can be designed by arranging a specific group of cells [13]. In QCA, the basic block is the majority gate as depicted in Figure 2, so that the rest of the gates can be derived from it. So, the researchers paid attention to this important block in terms of reliability, applications, and complexity with different inputs [14–23]. In addition to the majority gate, and to complete all the necessary functions, an inverter block, shown in Figure 3, is required. Circuit blocks can be connected using QCA-wire, accomplished with a chain of cells, as depicted in Figure 4 [12,24].

In addition to the above, it is necessary to provide a clock signal in order to control the flow of data and achieve synchronization to ensure that the results are correct. The QCA circuit that required a large number of cells can be divided into groups of zones where each zone contains four clock transitions (Relax–Switch, Switch–Hold,

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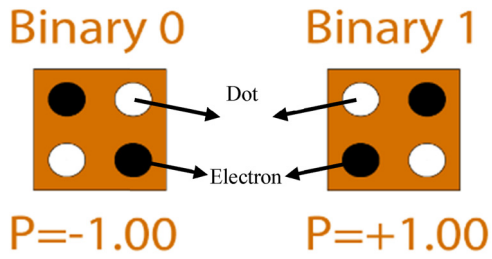

Figure 1: QCA cell configurations.

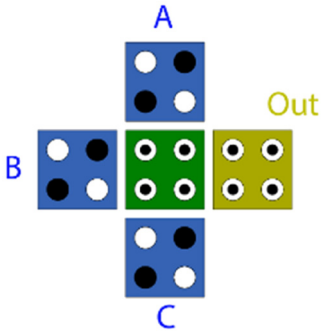

Figure 2: Cell configurations of majority block.

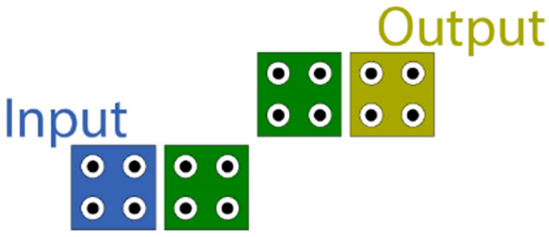

Figure 3: Cell configurations of inverter block.

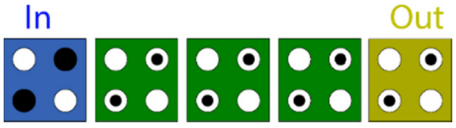

Figure 4: Cell configurations of QCA binary wire.

Hold–Release, Release–Relax) [25]. Figure 5 represents the clock signal that is commonly used in QCA technology.

3 Related work

The logic circuit can be designed using AND, OR, and NOR gates. There are other gates presented to simplify the circuit such as MUX and XOR. Previously, designing

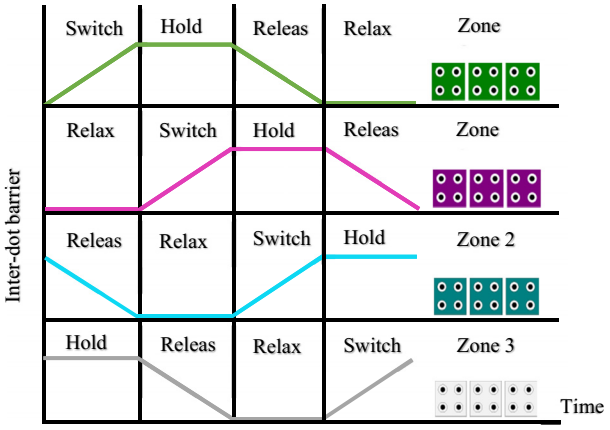

Figure 5: Clock signal zones and phases [26].

the XOR circuit using QCA technology faced the wire-crossing issue, as the main problem [27,28]. There are different attempts to implement XOR structure without wire-crossing [9,11,29,30]. However, all the prior implementations suffer from consuming a large area and delay (clock phases). These issues are attempted to be address in the current work. In 2015, Ajitha et al. [29] presented a new architecture of the QCA-XOR gate as depicted in Figure 6. This gate has many limitations where one of its inputs is not reachable in one layer and the design required three clock phases delay.

In 2016, Singh et al. [30] proposed a different layout of the QCA-XOR gate as shown in Figure 7. Although authors used it to construct an even parity generator, this gate required a high cell count and a three clock zones delay.

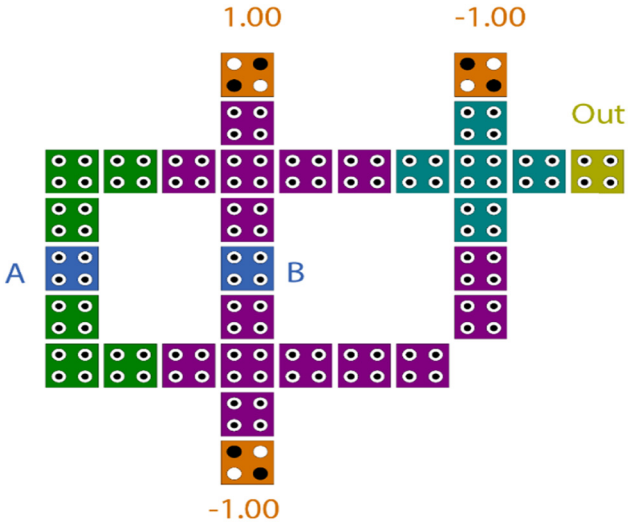

Figure 6: 2-input XOR gate proposed in ref. [29].

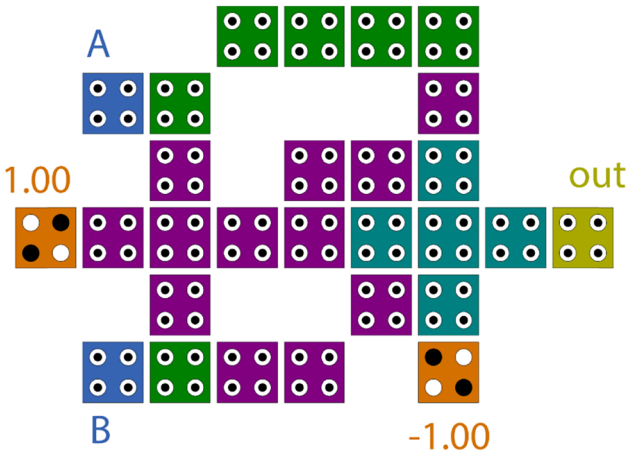

Figure 7: 2-input XOR gate proposed in ref. [30].

In 2017, Goswami et al. [9] suggested a new structure of 3-input XOR as shown in Figure 8. This gate was constructed based on 5-inputs majority voter. Although the suggested design takes two clock zones delay, it required a large cell count and it has an input not reachable in a single layer.

In 2018, Poorhosseini and Hejazi presented different structures of XOR gate in QCA form as shown in Figure 9 [11]. These two structures consume high cell count and four clock phases delay although the inputs can be accessed in a single layer.

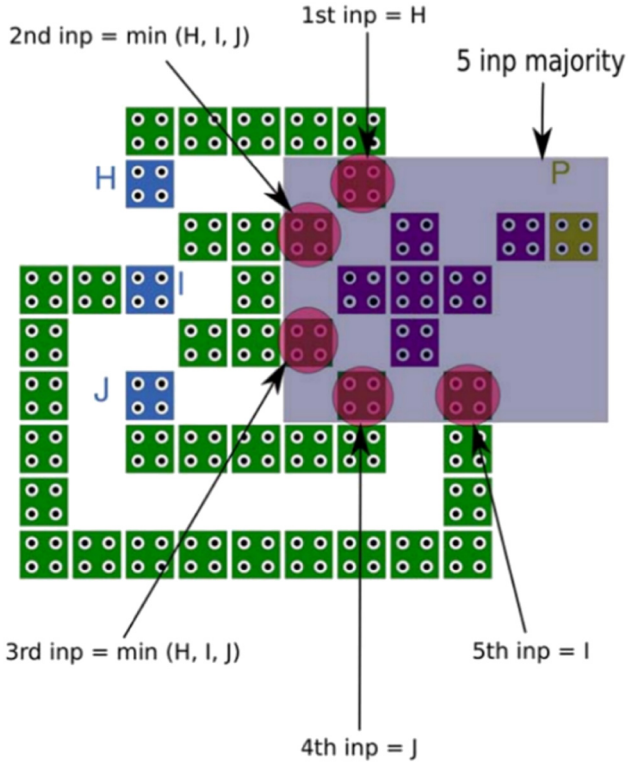

Figure 8: 2-input XOR gate proposed in ref. [9].

4 Proposed design

From the previous research related to QCA technology, the XOR gate has drawn attention due to its importance in digital systems. The currently available circuits regarding

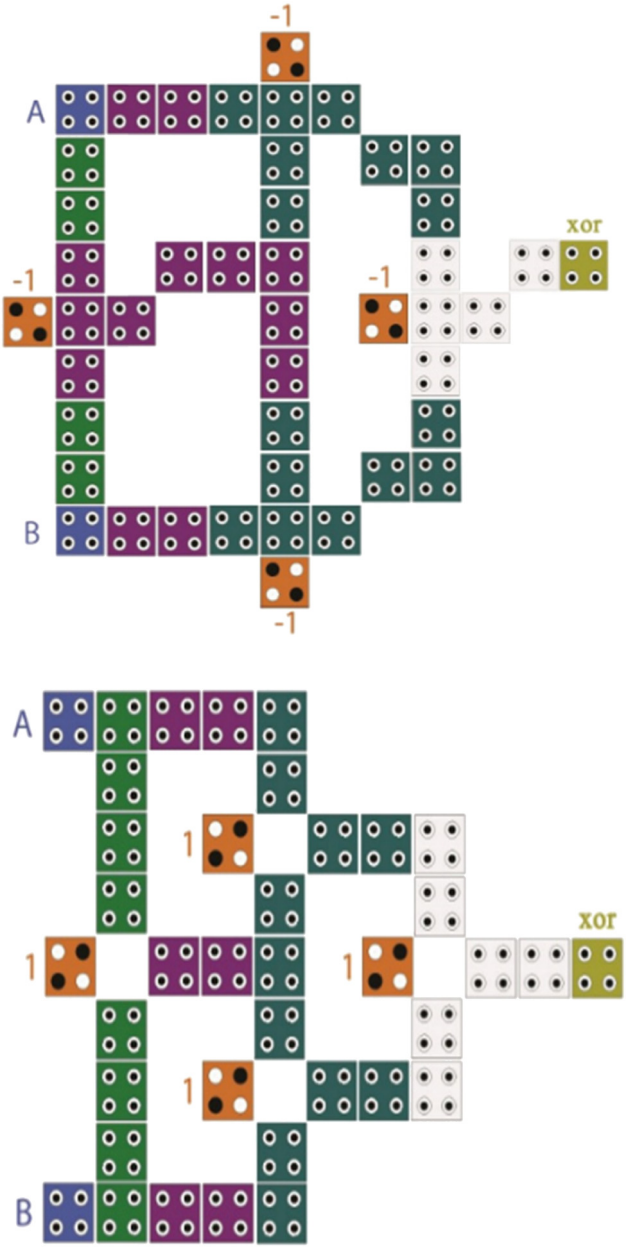

Figure 9: Different structures of 2-input XOR gate proposed in ref. [11].

Table 1: The functionality table of DFXOR

Selector (S)	A	B	C	Function	Output
0	0	0	x	A **XOR** B	0
0	0	1	x	A **XOR** B	1
0	1	0	x	A **XOR** B	1
0	1	1	x	A **XOR** B	0
1	0	0	0	A **XOR** B **XOR** C	0
1	0	0	1	A **XOR** B **XOR** C	1
1	0	1	0	A **XOR** B **XOR** C	1
1	0	1	1	A **XOR** B **XOR** C	0
1	1	0	0	A **XOR** B **XOR** C	1
1	1	0	1	A **XOR** B **XOR** C	0
1	1	1	0	A **XOR** B **XOR** C	0
1	1	1	1	A **XOR** B **XOR** C	1

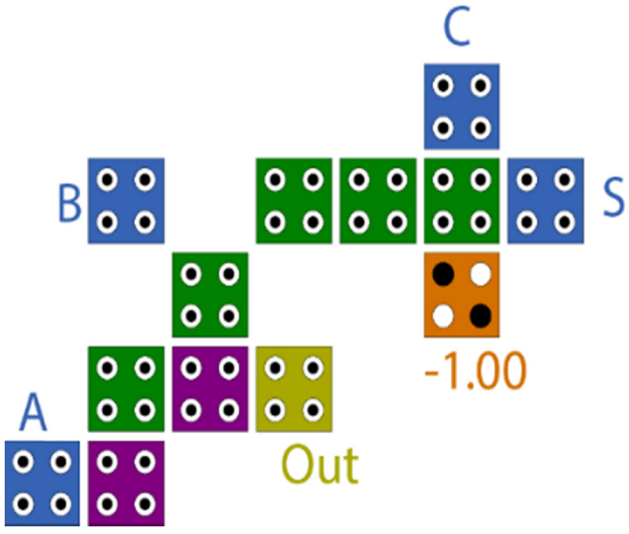

Figure 10: The QCA layout of the proposed gate.

the XOR gates are either with two inputs or with three inputs. In this research, a new Dual Function Block of XOR gate (DFXOR) will be presented. The DFXOR is the programmable XOR circuit in terms of choosing the number of necessary entries, as it works either as two inputs or as three inputs according to the selector (S). The truth table of the proposed circuit is detailed in Table 1. The QCA layout of the proposed gate is depicted in Figure 10. In QCA, the efficiency of a circuit could be measured by many metrics such as cell count, area, latency (delay), and cost. The proposed design is accomplished with noticeable values in all metrics where cell count, area, latency, and cost are 13, 0.01 μm^2, 2 clock phases, and 0.13, respectively. The cost of the circuit was calculated in the same manner as presented in ref. [31].

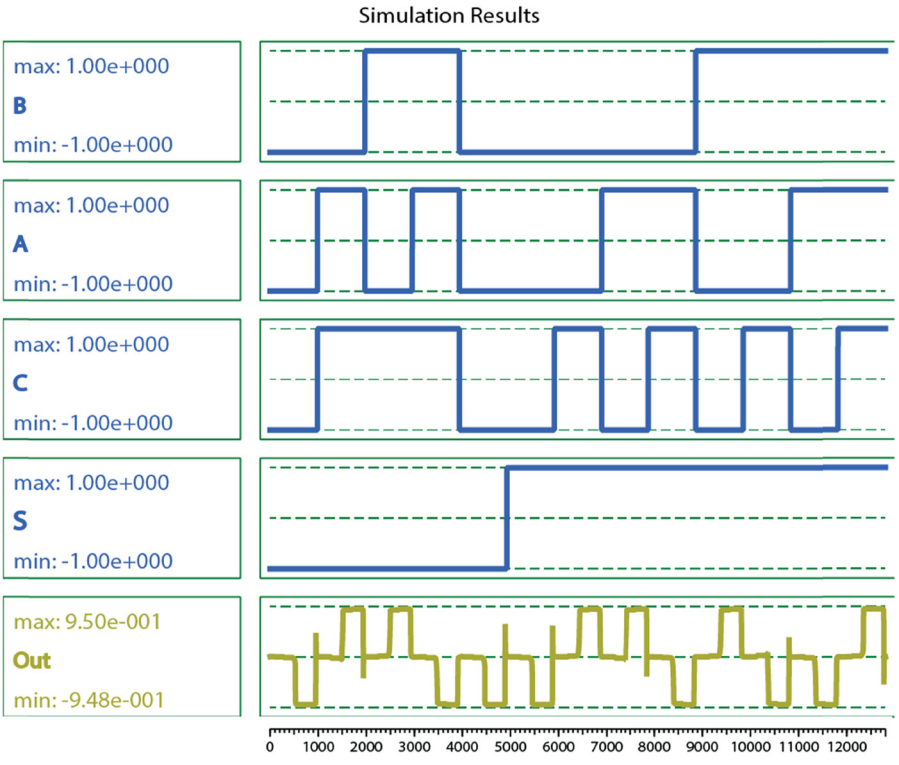

Figure 11: Simulation results of the proposed design.

Table 2: Result comparison table

Circuit	Area (μm^2)	Latency (clock phases)	Cell count	Cost (area × cell count)
2-bit XOR [32]	0.22	4	121	26.62
2-bit XOR [33]	0.17	6	115	19.55
2-bit XOR [34]	0.08	5	51	4.08
2-bit XOR [11] layout 1	0.05	4	45	2.25
2-bit XOR [11] layout 2	0.03	4	37	1.11
2-bit XOR [29]	0.04	3	32	1.28
2-bit XOR [30]	0.02	3	28	0.56
2-bit XOR [35]	0.02	3	28	0.56
2-bit XOR [35]	0.02	3	20	0.4
2-bit XOR [36]	0.01	2	14	0.14
3-bit XOR [27]	0.07	5	93	6.51
3-bit XOR [9]	0.04	2	47	1.88
3-bit XOR [37]	0.02	2	14	0.28
The proposed DFXOR	0.01	2	13	0.13

5 Simulation results and comparison

In this work, a dual-function block of the XOR gate is designed. The proposed design uses the intercellular effects to produce the output. The DFXOR has excellent features in terms of complexity, speed, and cost. The proposed gate was designed using the QCADesigner software Version 2.0.3. Using this free designing tool, the practical authenticity of the suggested designs has been confirmed. The following settings are modified using the coherence vector simulation engine as follows: cell size is set to 18 nm, and all other parameters are left at their default values. Figure 11 shows the input/output waveforms, where the blue color represents the input signals (A, B, and C) in addition to the selector (S) and the yellow color represents the output of the DFXOR. When the selector is connected to logic 0, the output equals (A XOR B), and when the selector is connected to logic 1, the output is (A XOR B XOR C). The results show that the proposed design is free of errors. From Table 2, it is clear that the proposed structure has competitive values in terms of complexity (area and cell count) in comparison with the same counterparts although it has a dual function. Compared with the previous 3-input XOR gates, which do not have the dual function, the results showed a significant improvement in terms of cell count, area, and cost by 7%, 50%, and 54%, respectively.

6 Conclusion

The XOR gate has attracted the attention of researchers, as it is used in many circuits in order to reduce its complexity. As the QCA technology is an emerging technology presented to replace CMOS technology, the researchers focused on designing different important circuits in this technology. In previous literature, many QCA-XOR structures have been proposed in different forms, some accepting two inputs, others three, as each design has a different performance and structure. The most previous designs suffer from consuming more area and cost. In this work, a dual-functional XOR gate is proposed. The proposed gate is simple and adapted to work either as a two-input XOR gate or a three-input XOR gate. The results obtained showed that the proposed block is effective and a strong competitor in terms of cost and area needed for implementation.

Conflict of interest: Authors state no conflict of interest.

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