Research Article

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Wide-dynamic-range high-conversion-efficiency rectifier circuit for 2.48 GHz RF energy harvesting

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Abstract: A pint-sized cross-coupled differential-driven rectifier (CCDDR) circuit with wide power dynamic range (PDR), and high power conversion efficiency (PCE) for 2.48 GHz LS-band RF energy harvesting is proposed. By building two novel functional modules of dynamic body-biasing assist (DBBA) and diode feedback biasing compensation (DFBC) into core rectifier, reverse leakage current while variation on gate potential and threshold voltage of core rectifier transistors can be effectively contained. Using 180 nm/1.8V RF-CMOS technology, the circuit design and layout are implemented. Followed by simulation-based performance comparison, the experimental results demonstrate that the proposed rectifier achieves a higher PCE of 77.8% at a lower input power of −12.5 dBm in 2.48 GHz frequency band. Additionally, benefiting from wider input PDR of 26 dB compared with other design cases, a single-stage topology rectifier can sufficiently yield a stable output supply voltage of high to 642.46 mV with the sensitivity at 1 V of −12 dBm, while the FoM value can be reached up to 54.52 dB, which can provide strong support for realizing source-free near-zero-energy-consumption IoT communication systems.

Keywords: radio frequency energy harvesting, differential-driven rectifier, power dynamic range, power conversion efficiency

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1 Introduction

Along with the rapid development of wireless sensor networks (WSN) and Internet of Things (IoT) technologies, there is a growing need for microelectronic devices on network nodes (Kumar et al. 2021), such as microsensors and tags, to operate continuously and over long periods of time. Traditional battery-powered method presents notable limitations, including frequent battery replacements and special peripheral operations in challenging and hazardous environments such as underground or underwater. These challenges not only inconvenience users and operational personnel but also escalate the operating costs. In terms of these issues, the wireless radio frequency (RF) energy harvesting technology, as an emerging alternative to traditional batteries, has become one of the most promising technologies of source-free power supply and power management systems. This shift has prompted significant interest in device and circuit design techniques in energy harvesting, making it a focal point of research in the field (Chen et al. 2020, 2021, Ruan et al. 2017).

Commonly, energy sources harvested from the natural environment can be classified into solar energy, thermal energy, vibration energy, and RF energy (Zhu et al. 2022). In comparison with other energy sources, the unit energy harvesting capacity from RF signal during wireless communication is relatively lower, only about the microwatt level. However, RF energy exhibits distinct advantages compared with other energy sources. Apart from serving as a signal carrier (also known as local oscillator, LO) medium for source-free IoT communication, RF energy has superior features in terms of wide-range applicability, energy transmission capabilities, real-time functionality, continuity, sustainability, and multi-source energy harvesting (Ijala et al. 2022, Panigrahi et al. 2021, Pullwitt et al. 2022, Sanislav et al. 2021). These advantages indicate broad prospects for the application of RF harvesting technology in current hot areas such as WSN, IoT, wearable devices, and micro-robots (Yahya Alkhalaf et al. 2022, Liu et al. 2017, Moloudian et al. 2024).

RF energy harvesting technology involves converting ambient wireless RF signals into electric energy, which serves as the power source for sensors, tags, and microelectronic devices within IoT network nodes (Eshaghi and Rashidzadeh 2020). This technology is widely recognized for offering a viable solution for self-sustaining power supplies in microelectronic devices and wireless communication systems (Correia and Carvalho 2016, Kim et al. 2019, Merakeb et al. 2022). As one of the most core components in RF energy harvesting system, a high-performance rectifier circuit is mainly designed to convert high-frequency AC signals into stable DC power supply voltage. Consequently, enhancing the rectifying efficiency becomes crucial in meeting requirements in terms of diverse power supply voltage, stability, and response rate for various circuit loads (Chun et al. 2022). Thus, improving performance of the rectifier circuit in these aspects is a key topic to achieve high-efficiency energy harvesting technology. Figure 1 illustrates a generic RF energy harvesting architecture, which includes an antenna for receiving RF signal, an L-type passive impedance matching circuit, a core rectifier module, and a back-end energy storage/management unit. This architecture is employed for performance verification in this study.

Two commonly used circuit topologies of rectifier for RF energy harvesting include Dickson-type (Zheng et al. 2024) and cross-coupled differential-driven type (ur Rehman et al. 2017). The cross-coupled differential-driven rectifier (CCDDR) utilizes a couple of differential signals to drive the rectifier, which can effectively suppress common-mode noise, improve anti-interference ability during the AC-to-DC conversion, resulting in stability of final output supply voltage. Compared with the Dickson-type, CCDDR has a better low-voltage start-up feature, which can benefit more efficient rectification even at weak input power. Additionally, it often operates in high-speed circuit, making it suitable for high-frequency signal receiving and transmitting system environment.

Gate-biasing and body-biasing are the most effective means to optimize the performance of rectifiers. Lau and Siek (2017) employed a novel DC-boosted biasing technique to efficiently address the issues of diode forward voltage drop, forward peak current, and reverse leakage current. Lian et al. (2022) innovated a novel gate-biasing technique by setting coupling capacitors at each stage for better biasing of subsequent stage, and achieved an improved sensitivity of −20 dBm at 1 V output. Noghabaei et al. (2022) proposed a dynamic and static bias compensation technique to lower the effective threshold voltage for a 10-stage cross-connected rectifier topology, resulting in a better sensitivity at 1 V output of −25.5 dBm and input power range. Moghaddam et al. (2017) employed the lower DC feeding (LDCF) combining self-body-biasing technique in far-field REHS to enhance PCE, which allows PMOS transistors to operate with dynamic threshold voltage for better PCE and output performance at a smaller input power level. Park et al. (2023) adopted body-isolated MOSFETs with deep-n-well body-biasing technique to manipulate the highest reverse bias for minimizing the leakage current, resulting in the improved features in terms of PCE, output voltage, and PDR. Chong et al. (2021) also presented a CCDD rectifier featuring a self-body-biasing combining two input–capacitor-coupling configuration technique, which reduces the forward threshold voltage and reverse-leakage current effectively. Almansouri et al. (2018) proposed an RF-to-DC power converter with variable biasing technique to selectively switch on/off the rectifying transistor, resulting in an 86% PCE and −19.2 dBm sensitivity when operating at the medical band 433 MHz with a 100 kΩ load. These studies indicate that improvement on gate or body bias of MOS rectifying transistors can effectively enhance the rectification effect. In this design case, both aspects of gate-biasing and body-biasing are employed simultaneously to achieve the optimal performance.

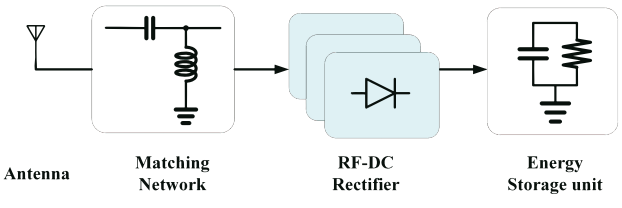

Figure 1: Block diagram of an overall RF energy harvesting system. Source: Created by the authors.

Aiming to meet requirements of battery-free ultralow-energy-consumption application for modern wireless communication systems, this study presents a novel self-biased CCDDR circuit with advantages on wide input power dynamic range (PDR) and high power conversion efficiency (PCE). The main contributions are summarized as follows:

(1) We propose a novel diode feedback biasing compensation (DFBC) module to contain the reverse leakage current while stable gate voltage of core rectifier transistors effectively enhances PCE;
(2) We propose an ingenious dynamic body-biasing assist (DBBA) module to mitigate substrate bias variation to stable threshold voltage while improving anti-noise interference feature;
(3) We implement back-end design of the proposed rectifier with compact size by 180 nm/1.8V RF CMOS technology while demonstrating obvious improvement and significant advantages in PCE and PDR.

The rest of this article is organized as follows: Section 2 presents the CCDDR and introduces the design details of the DBBA function module and DFBC module. Section 3 demonstrates Cadence-based pre-/post-layout simulation results, comparative analysis, and discussions. Section 4 covers the back-end layout implementation and simulation performance verification. Finally, conclusions and future works are provided in Section 5.

2 Design and optimization

2.1 Traditional CCDDR

Figure 2(a) displays the conventional single-stage CMOS CCDDR in basic single-stage bridge topology that receives RF differential signals through two input terminals (ur Rehman et al. 2017).

In the initial operating phase, if input signal V_{RF}+ falls within the "positive half-cycle" of an ideal AC sin stimulus, the node voltage V_x becomes positive while V_y becomes negative, with $V_x = -V_y$. Subsequently, the gate-source voltage of transistor MN2 is calculated as $(V_x - V_y)$, resulting in $2V_x$, which signifies that MN2 is in a sufficient conducting on state. Compared to the traditional single-ended input Dickson charge-pump rectifier circuit (Schmickl et al. 2020), as shown in Figure 2(b), the gate-source voltage of core rectifier transistor MN2 or MP1 can be widened twice than that of the Dickson's, thereby creating more favorable conduction conditions to harvest the weaker signal energy. As a consequence, the CCDDR circuit with a complete symmetry topology can operate effectively at a lower input voltage level (V_{RF}). This feature indicates an enhanced ability to detect and receive weak RF signals present in the environment, thus boosting its overall sensitivity.

In the meantime, due to this cross-coupled topology, MP1 experiences a gate-source voltage decrease to $(V_x - V_y)$, i.e., $-2V_x$, resulting in MP1's activation. Consequently, it means the "effective turn-on voltage" of MP1 is also reduced at that moment. Therefore, as a summary, during the positive half-cycle of V_{RF}+, MN2 charges energy-harvest capacitor C_{EH2} from ground on the left, while MP1 charges the load capacitor C_{L3} from energy-harvest capacitor C_{EH1} to the output terminal. Under this operation phase, a rectifier circuit can sufficiently harvest RF signal energy and then convert it to DC voltage while storing into the energy-harvest capacitor. It should be noted that both MN1 and MP2 are in the optimal high-voltage sub-threshold operating state (approximate cut-off state), which can effectively contain the reverse leakage current to maintain high energy conversion efficiency.

On the other hand, in "reverse" operating phase when V_{RF}+ turns to the "negative half-cycle" of AC signal, MN2 and MN1 switch working roles as well as MP1 and MP2. It charges from ground to C_{EH1} via MN1 that is switched on, while it charges from C_{EH2} to C_{L3} via MP2. It means that, in every half cycle, the rectifier circuit consistently charges the grounded terminal toward energy-harvest capacitor while energy-harvest capacitor on the other side toward output load capacitor. Based on this differential-driven input rectifier topology, and the energy harvesting approach in time-division of positive and negative clock

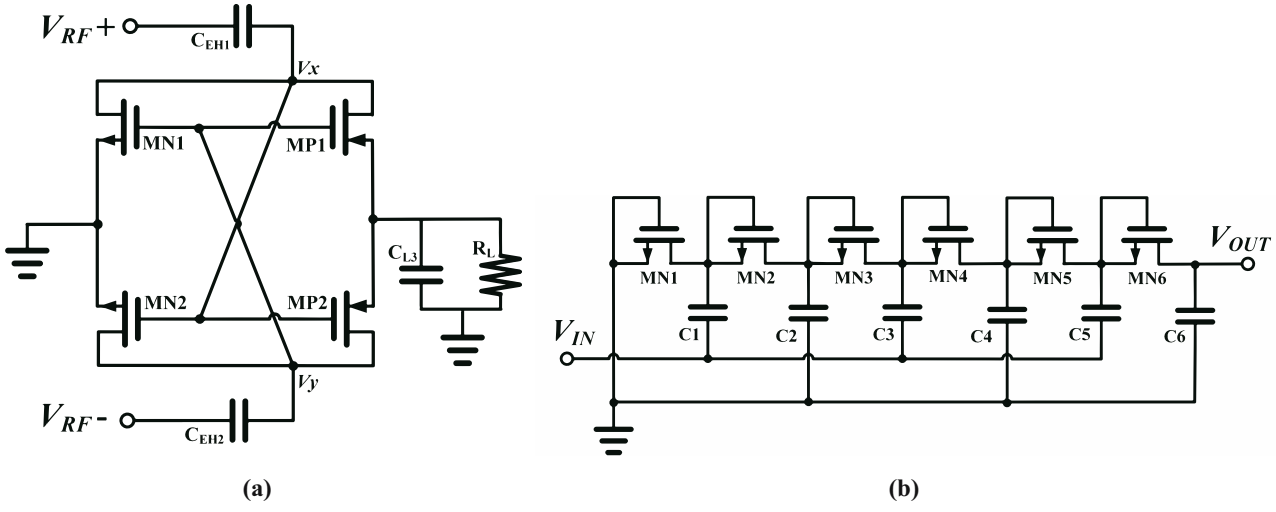

Figure 2: (a) Conventional single-stage cross-coupled differential-driven CMOS rectifier and (b) three-stage single-ended input Dickson charge-pump rectifier. Source: Created by the authors.

cycles, it greatly enhances the energy conversion and storage efficiency especially to the low-power RF signal source.

2.2 Proposed improved rectifier circuit

Figure 3 shows the improved single-stage CCDDR circuit we proposed. It incorporates two feature points. One is the DFBC module, which is cross-connected to the gates of two N-type rectifying MOSFETs. The other is the DBBA module, which is connected symmetrically to the bulks (substrates) of two P-type rectifying MOSFETs. In this topology strategy, the former stabilizes the gate voltage of core NMOS rectifying transistor and contains the reverse leakage current, while the latter lowers the effective threshold voltage of PMOS rectifying transistor and mitigate the substrate-bias variation. This combination can effectively achieve stabler and more efficient turn-on and -off of the rectifying transistors, ultimately to optimize the energy conversion efficiency while enhancing PDR from input RF power to output DC supply voltage.

2.3 DFBC

For design implementation of a DFBC module, as illustrated in Figure 4, first, four high-threshold-type PMOS transistors MP3, MP4, MP5, and MP6 are constructed as the equivalent-diode-connection topology. And then, MP3 and MP4 that connect in series act as an equivalent diode D1, while MP5 and MP6 act as D2. The anodes of two equivalent diodes are

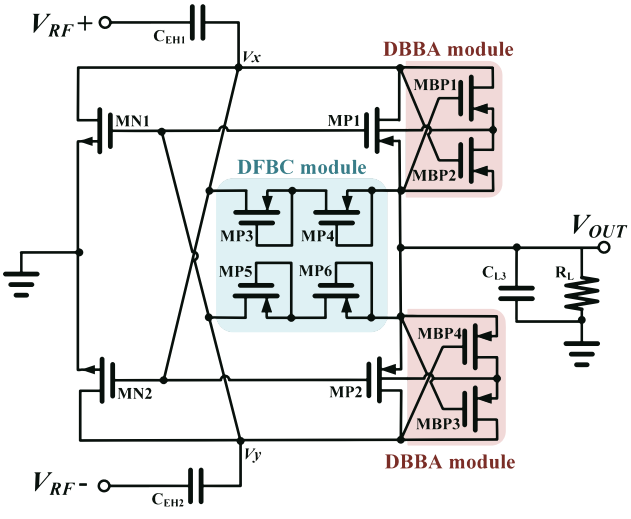

Figure 3: Proposed improved single-stage CCDDR. Source: Created by the authors.

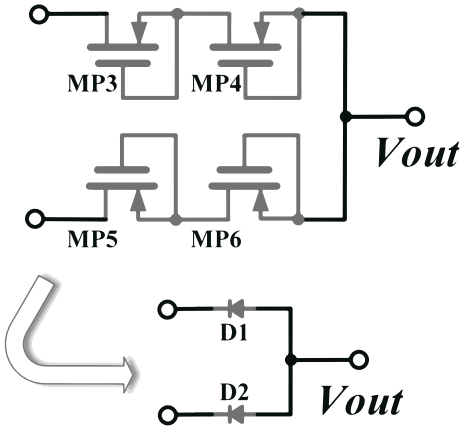

Figure 4: Equivalent model of DFBC module for PCE and PDR improvement. Source: Created by the authors.

shorted and connected to the output of the rectifier circuit. However, as shown in Figure 4, two cathodes of D1 and D2 cross-connect to the four core rectifying NMOS transistors MN2–MP2 and MN1–MP1, respectively.

As the first advantage, via the cathode potential of equivalent diode, this topology configuration enables rectifier circuit to provide a signal (energy) loop to form a positive feedback, which biases in turn and regulates adaptively the gates of four core-rectifying transistors. This feedback loop provides continuously a high voltage that be fed back by output onto the transistor gate to counteract the threshold voltage; it means that once the initial energy harvesting action starts up, the four core rectifier transistors will be in always-on working state. Since it avoids the loss of threshold voltage caused by turning on the rectifying transistors during the on/off device switching process, this proposed feedback topology bridging between in and output can significantly improve the energy conversion efficiency.

On the other hand, compared with the single-ended input Dickson rectifiers, a differential-input rectifier circuit generally represents larger reverse leakage current, due to the more signal flowing paths based on its double-ended input cross-coupled topology. Here, as the second key feature, utilizing high-threshold-type MOS transistor as the feedback equivalent diode will benefit in containing the reverse leakage current while efficiently harvesting high-input-power RF signals. A higher threshold voltage makes it more difficult to switch on the transistors; thereby, it means an increased equivalent on-resistance between the drain and source. Even though an equivalent diode is reversely biased by the reverse leakage current, the flowing reverse leakage current can be effectively reduced and suppressed due to the larger on-resistance.

The design approach mentioned earlier effectively suppresses the reverse leakage current while stabilizing the gate voltage of the core rectifying transistors, which improves the PCE feature. As shown in Figure 5, once the PCE is improved, the sensitivity to a weak input power of RF signal will also be enhanced, i.e., the input dynamic harvest range of the overall rectifier circuit will be effectively improved accordingly along with increased PCE value. Furthermore, it should be noted that the proposed single-stage differential-driven rectifier in this study can be further expanded to a multi-stage topology by cascade-connection, and the controllable input-power PDR can also be widened as reported in some similar previous studies (Alhoshany 2022, Lau et al. 2020, Wong et al. 2019).

2.4 DBBA

For the design implementation of a DBBA module, as illustrated in Figure 6, two additional auxiliary PMOS transistors, MBP1 and MBP2, are shorted in their sources, while two drains are further connected to the source and drain of the core rectifying P-type transistor MP. This handling manner targeting of substrates of two core rectifying PMOS transistors contributes to regulate the body-bias potential strategically of the core transistors that are on main charging transporting (charging process) path (Al-Absi et al. 2021, Chun et al. 2022).

The working principle of dynamic body-biasing for improving PCE feature is described as follows: one auxiliary transistor MBP1 shorted-connects the source-end and substrate with core transistor MP, while the other MBP2 shares the same drain-end and substrate. During the positive half cycle of AC signal of V_{RF}+ input, as demonstrated in Figure 3,

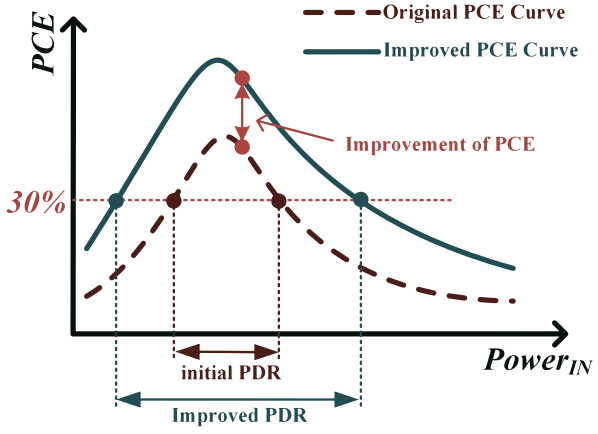

Figure 5: Widened PDR along with the improvement on PCE feature. Source: Created by the authors.

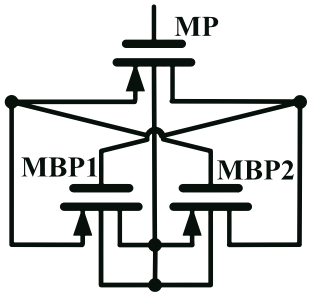

Figure 6: Diagram of DBBA function module for restraining reverse leakage current. Source: Created by the authors.

both MP1 and MBP1 are switched on concurrently. By promptly forming an equi-potential due to the short-circuiting on source and substrate of MBP1 and MP1, respectively, the reverse bias voltage between source-end and substrate of MP1 can be counteracted. It means that, by mitigating the body effect in such manner, the voltage loss induced by increase (and fluctuation) of the threshold voltage on rectifying transistor MP1 can be prevented effectively.

Conversely, once V_{RF}+ input turns to the negative half-cycle, MP1 and MBP1 are switched off, while the anti-leakage auxiliary transistor MBP2 conducts on. Consequently, by short-circuiting the drain-end and substrate of MP1 and MBP2, the operating issues due to the floating substrate of MP1 such as the mis-bias of substrate and noise interference would be solved effectively to further ensure stable and efficient operation of the rectifier circuit. As a simple summary, in essence, this novel DBBA functional topology we proposed for core PMOS pair serves to effectively suppress the additional turn-on power consumption arising from threshold voltage fluctuation of PMOS transistor, thereby enhancing PCE of the overall rectifier circuit.

3 Sizing and analysis

Based on 180 nm/1.8 V RF CMOS technology, both of the front- and back-end designs of the proposed rectifier circuit, as well as simulation-based performance analysis, are performed. Table 1 lists all the channel sizes of MOS transistors and the parameter values of passive capacitors and resistor used in rectifier circuit design.

3.1 Feature of single-stage rectifier

Considering the requirement of LS-band wireless communication, the performance analysis is carried out under

Table 1: Design parameters of the proposed rectifier circuit

Device	Size (W/L)/value	Device	Size (W/L)/value
MN1	6.6 μm/180 nm	MBP1	11.5 μm/180 nm
MN2	6.6 μm/180 nm	MBP2	11.5 μm/180 nm
MP1	39.36 μm/180 nm	MBP3	11.5 μm/180 nm
MP2	39.36 μm/180 nm	MBP4	11.5 μm/180 nm
MP3	26 μm/180 nm	$C1$	1.13 pF
MP4	26 μm/180 nm	$C2$	1.13 pF
MP5	26 μm/180 nm	$C3$	1.13 pF
MP6	26 μm/180 nm	R_L	10KΩ

2.48 GHz frequency input. During the AC-to-DC energy conversion of the RF signal, the output voltage, PCE and PDR are three key performance metrics for evaluating the proposed rectifier circuit.

First, we investigate the suppression effect on reverse leakage current by adding the DFBC module. Taking a core rectifying transistor MN1 (as well as MP1 in Figures 2(a) and 3) as the observation object, Figure 7 shows the transient changing trend of its gate current. It can be seen that, benefiting from the DFBC module, the gate current of the core rectifying transistor represents an obvious increase in amplitude by more than 216 μA in each positive or negative half-cycle, which confirms that the reverse leakage current is effectively contained to a large extent after the topology improvement.

Next, to simulate a more realistic energy harvesting environment, we set −12.5 dBm (equivalent to 0.056 mW, as a normal test signal intensity in 2.48 GHz IoT RF communication) as input power and run the transient

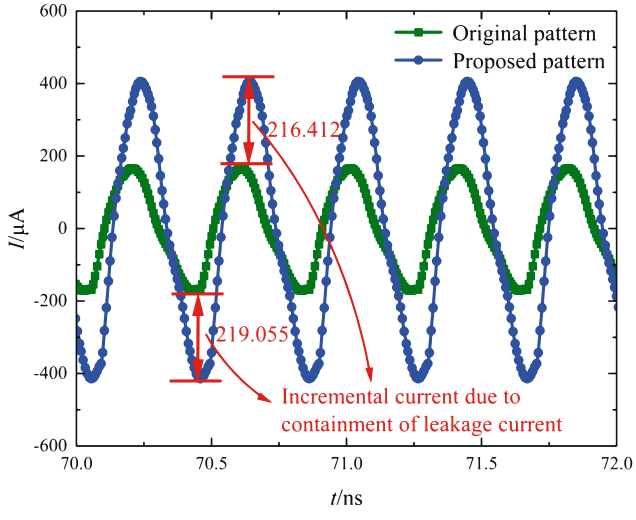

Figure 7: Increased gate current of rectifying transistor MN1(MP1) before/after topology improvement. Source: Created by the authors.

simulation to observe the output voltage curve. As shown in Figure 8(a), compared with the original traditional rectifier circuit before optimization, the improved rectifier circuit demonstrates a notable enhancement. The average voltage in stable output status of the proposed rectifier can reach up to 642.46 mV, which marks a significant improvement of 27% over the non-improved pattern's 505.94 mV.

Additionally, Figure 8(b) presents the sampled results of PCE across input power range from −30 to 10 dBm. The plot result reveals that, due to the reduction of the energy loss induced from the leakage current, the proposed rectifier could achieve a maximal PCE value of 77.8%, with 4.08% increase over the peak efficiency of 73.7% in original non-improved pattern. Furthermore, according to the calculation manner of PDR (namely, input power range), as illustrated in Figure 5, assuming that it is evaluated based on a common criterion of PCE > 20%, as shown in Figure 8(b), the PDR after improvement can be determined as 26 dB, which also has advantages of 1 dB over the unoptimized original pattern.

Moreover, under different load conditions including 1 kΩ, 3 kΩ, 10 kΩ, 100 kΩ, and 1 MΩ, the feature experiments in terms of the output voltage level and the PCE at 2.48 GHz are implemented. Figure 9(a) illustrates the simulated average V_{OUT}, while the corresponding PCE plots are shown in Figure 9(b). Remarkably, once beyond the optimum load resistance for each input power, further increase in load resistance would result in the degradation of PCE due to the decreased output power as well as the dominated power dissipation in rectifying elements. As relatively good two load points at 10 and 100 kΩ, the proposed rectifier exhibits a stable output feature with voltage levels of 642.46 and 842.49 mV, respectively. For R_L = 10 kΩ, PCE above 20% can be achieved with a wider input PDR from −21 to 5 dBm, with peak PCE of 77.78% at −13 dBm input power. Then, for R_L = 100 kΩ, PCE above 20% can be achieved with a narrow input PDR from −24 to −12 dBm, but with an optimal peak PCE of 79.97% at −19 dBm input power, which makes it applicable when we consider subsequent device connection such as a level shifter, low-dropout (LDO) regulator (Liu et al. 2022, 2024), or a DC-DC converter in actual ambient RF energy-harvesting (RFEH) systems.

3.2 Feature of multi-stage rectifier

Focusing on the goal of achieving a higher power supply voltage close to stable 1 V output, which cannot be reached due to the limitation of energy conversion capability of single-stage topology, thereby a multiple double-stage

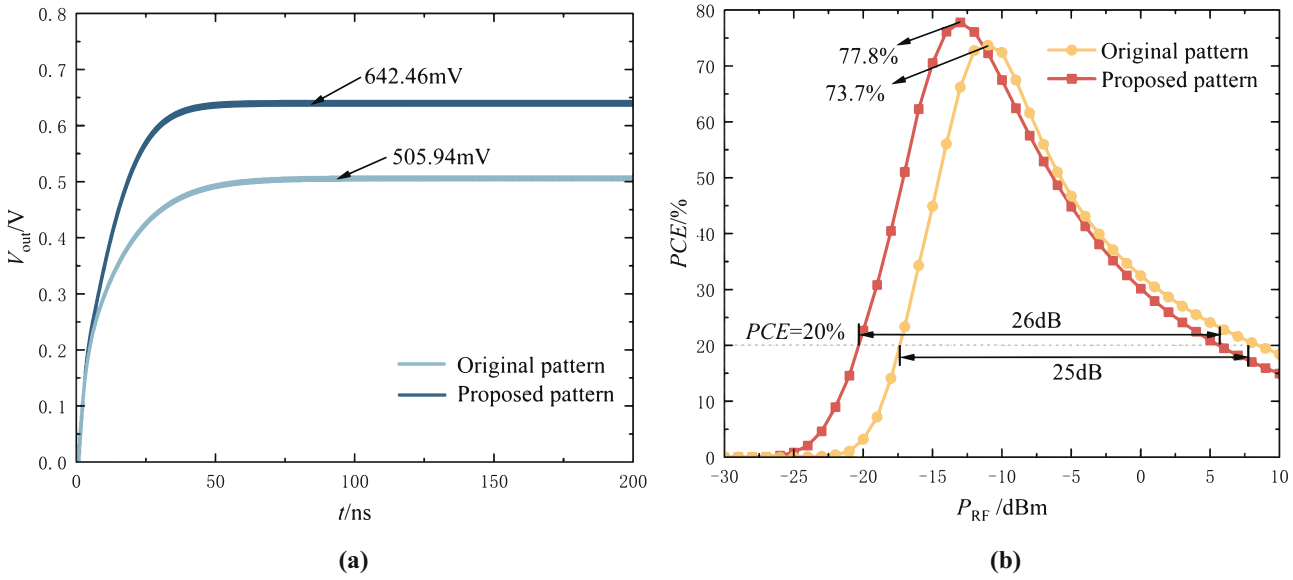

Figure 8: Feature comparison before/after improvement: (a) average output voltage under an input power of −12.5 dBm and (b) enhanced PCE. Source: Created by the authors.

cascade CCDD rectifier is designed, as shown in Figure 10. The circuit performance analysis is carried out under the same stimulated condition as previous single-stage pattern. The graph clearly shows significant enhancements in output voltages, by cascading two or more single-stage modules to construct a multi-stage rectifier chain.

Figure 11(a) presents the transient simulation-based curve comparison in terms of output voltage, for the proposed single-stage and double-stage rectifiers, under input powers of −6 dBm (notably, the multi-stage rectifier is more sensitive to input power above −6 dBm) and the higher −4 dBm, respectively. Also, surely, for two stimulated signals with different input power (input signal intensity) of −6 and −4 dBm, the capability of converting and boosting up the output voltage is also different.

For pattern of −6 dBm input power, the converted average output voltage increases from 1.05 to 1.41 V (Curve #1 in single-stage to Curve #2 in multi-stage in Figure 11(a)), which represents remarkably enhancement of almost 40% by extending to multi-stage cascade topology. Similarly, for a higher input power of −4 dBm, the output voltage can be boosted up from 1.18 to 1.54 V

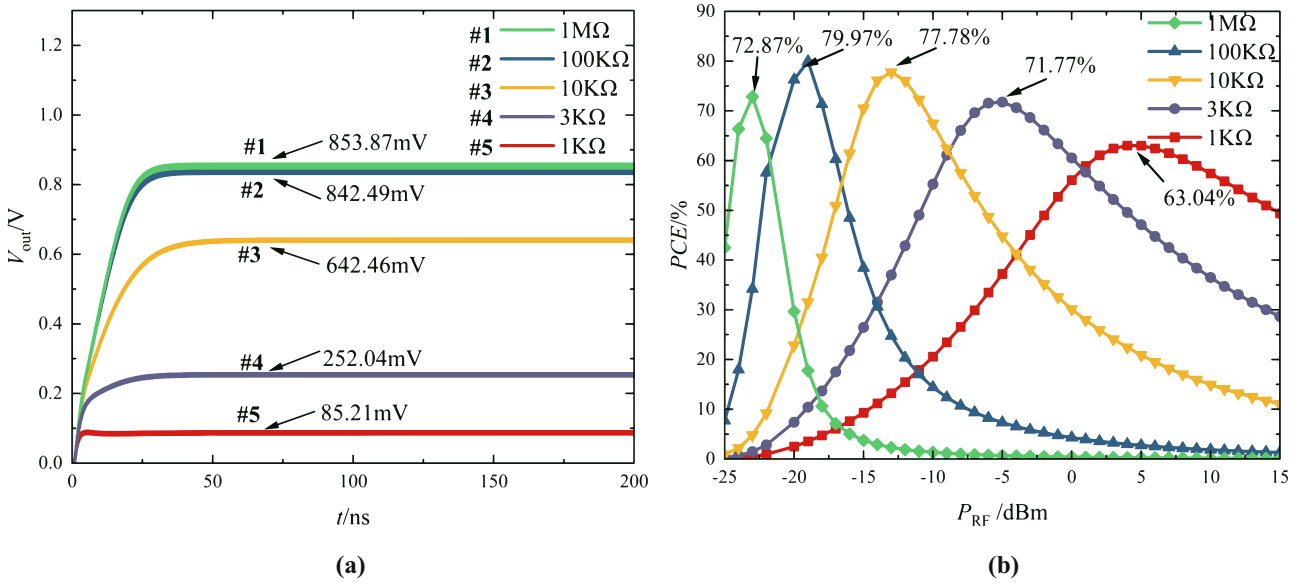

Figure 9: Comparison of the load-driving characteristic of the improved rectifier under different output loads: (a) average output voltage and (b) PCE. Source: Created by the authors.

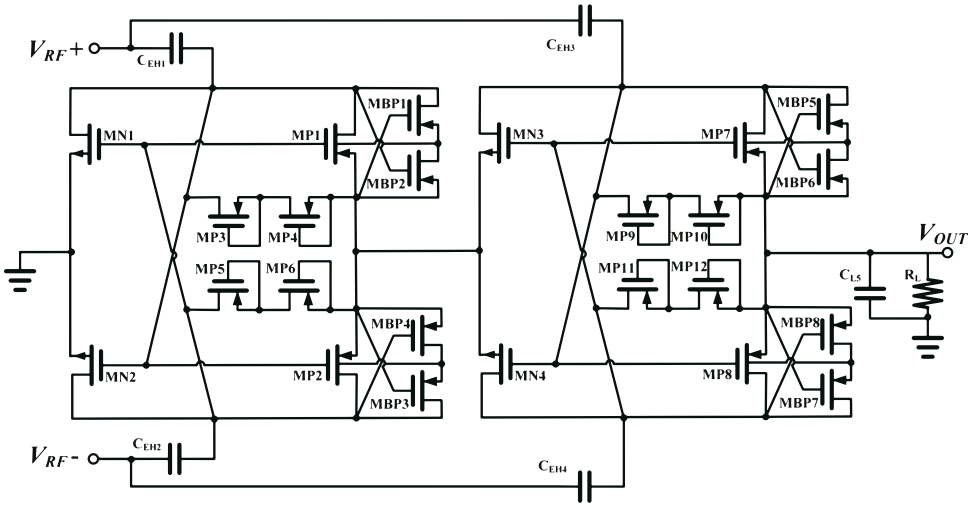

Figure 10: Proposed double-stage cascade CCDDR. Source: Created by the authors.

(Curve #3 to Curve #4), also representing a notable improvement of 30.5%.

Figure 11(b) shows the varying trends in PCE of single-stage and multi-stage patterns as the input power varies from −30 to 10 dBm. First, regardless of that how the input power or cascade stage varies, the peak PCE values of four rectifier patterns are limited in maximum by around 77%. Under the stimulated condition of −6 dBm input power, the maximal PCE values are 77.6 and 76.1%, for the single-stage and multi-stage rectifiers, respectively, whereas for −4 dBm, the values stand at 77.7 and 76.7%. Furthermore, no matter which input power of −6 or −4 dBm is simulated for PCE, both of the single-stage and double-stage patterns show a significant increase and feature enhancement in PDR, i.e., can gain a wider input power range, on a greater PCE level of 30% (compared with previous PCE > 20%) for estimation, which serves as a benchmark for common comparison in this study. As noted especially in −6 dBm input power case in Figure 11(b), obviously, compared with the single-stage pattern, a significant increment from 15 to 20 dB, almost 5 dB can be obtained by cascading as double-stage rectifier and 8 dB improvement at −4 dBm driven input power.

3.3 Comparison and discussion

A performance comparison of the proposed single-stage CCDDR with other similar design cases is made, mainly

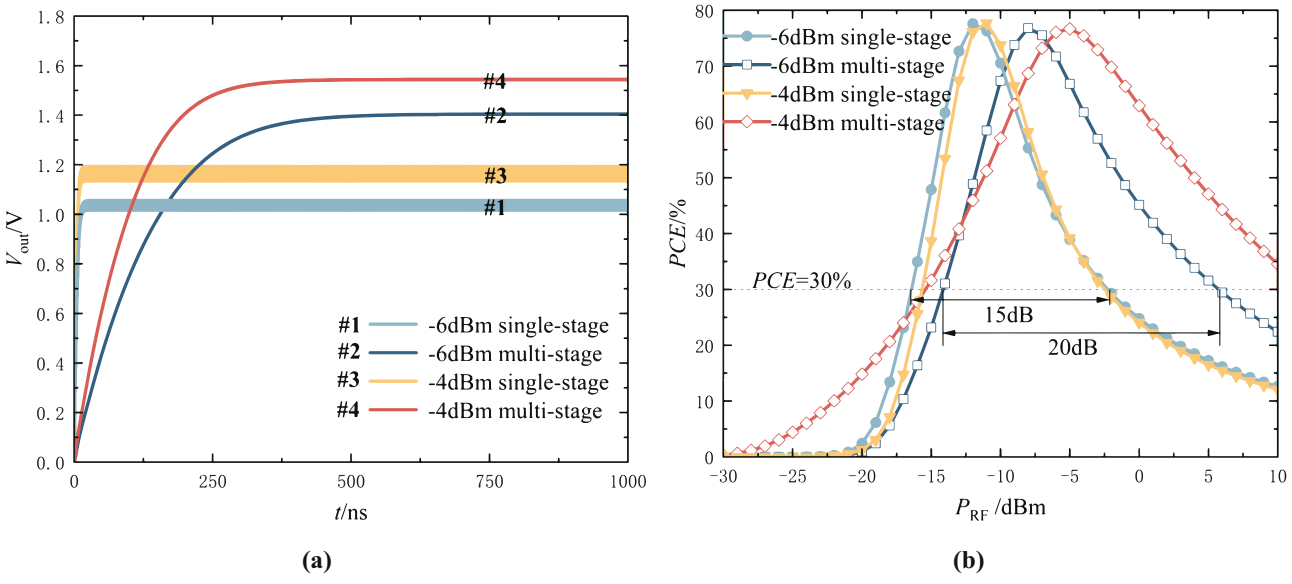

Figure 11: Comparison between single-stage and double-stage by two different input power stimulates of −6 and −4 dBm: (a) average output voltage level and (b) PCE. Source: Created by the authors.

Table 2: Performance comparison of rectifier circuit with other design cases

Item/ Parameter	2017' (Lu et al. 2017)	2024' (Nagaveni et al. 2024)	2019' (Xu et al. 2019)	2020' (Nagaveni et al. 2020)	2023' (Choo et al. 2023a)	2023' (Churchill et al. 2023)	2023' (Choo et al. 2023b)	2023' (Lian et al. 2023)	2024' (Argote-Aguilar et al. 2024)	This work	
Process node (nm)	65 CMOS	180 CMOS	65 CMOS	180 CMOS	65 CMOS	130 COMS	130 CMOS	65 CMOS	Schottky diodes	180 CMOS	
Operating frequency (GHz)	0.9	2.4	2.45	2.4	0.9	0.9	0.9	0.9	0.889	2.48	2.48
Input power (dBm)	−10	—	−3	−16	—	—	—	—	—	−12.5	−6
Stage number	5	3	1	3	3	3	3	3	2	1	2
Load impedance (kΩ)	147	—	—	5	100	100	100	100	—	10	10
Output voltage (V)	2	—	0.85	1	—	—	—	—	—	0.64	1.41
Peak PCE (%)	⊛36.5	⊛40	⊛48.3	⊛43.1	⊛79.77	⊛47.91	⊛78.4	⊛88.7	⊛63	77.8/⊛64.2	77.6
PDR (dB) (@PCE>20%)	⊛11	*⊛18	*⊛11	*⊛16	⊛19	⊛22.8	⊛19.5	⊛23	*40	26/⊛15	27
Sensitivity at 1V	−21 dBm for Rs = 1.2kΩ	−28 dBm Rs = ∞	* − 1 dBm for Rs = 100 kΩ	* − 14 dBm for Rs = 100 kΩ	−15.5 dBm for Rs = ∞	−21 dBm for Rs = 1 MΩ	−18 dBm for Rs = 100 kΩ	−21 dBm for Rs = 1 MΩ	—	−12 dBm for Rs = 100 kΩ	−16.85 dBm for Rs = 100 kΩ
Circuit area (mm^2)	0.048	—	—	—	0.023	0.18	0.095	0.028	—	0.00532	—
FoM (dB)	14.29	7.15	6.2	11.39	1.81	8.21	11.49	15.34	—	54.52/⊛25.96	28.24

Note: * Estimated from the figure; ⊛ Post-layout simulation results.

in terms of output voltage level, peak PCE, PDR, sensitivity, and layout dimension, of which the detailed parameter results are listed in Table 2. It can reveal that for an operating frequency of 2.48 GHz, and under similar or even lower input power of −12.5 dBm with load impedance of 10 kΩ, first, the proposed rectifiers realize the highest PCE of 77.8% in single-stage and 77.6% in double-stage pattern, respectively. Meanwhile, although the converted DC output voltage level for single-stage is only 0.64 V, the double-stage pattern by adopting a cascade topology can further boost the level up to over-doubled 1.41 V. Additionally, our proposed rectifiers represent that the PDR, i.e., the perceivable input power range where the PCE > 20%, can be reached to 26~27 dB in both single- and double-stage patterns, which shows significantly obviously superior compared with the most designs among ten cases. Furthermore, as illustrated in Figure 12, according to the analysis approach in Lu et al. (2017) and Nagaveni et al. (2024), a sensitivity factor that is generally defined as the minimum input power at which the rectifier can harvest and output a 1 V DC voltage in nowaday low-power application, can be measured as to be −11.89 dBm in our design case.

Finally, to provide a fair, comprehensive evaluation regarding to the all ten design cases, a figure of merit factor (FoM) (Choo et al. 2022, Chun et al. 2022) is further calculated with the key feature parameters to fairly and visually reflect the all-sided performance of our proposed rectifier, which is expressed as follows:

$$\mathrm{FoM} = \frac{\mathrm{PCE} \times \mathrm{PDR}}{N} \times \log_{10}\left(\frac{f_c}{f_0}\right), \tag{1}$$

where N is the total stage number of multistage rectifier circuit, f_c is the central operating frequency, and f_0 = 5 MHz is the frequency normalization factor, which is adopted to uniformly evaluate the performance of the state-of-the-art rectifiers operating in different frequency. The final results are listed in Table 2, and it can be observed that our easy-to-extend rectifier has the best FoM value of 54.52 dB among all the comparable ten design cases. These comparison results prove that our topology optimization approach on the single-stage CCDDR is effective and applicable for built-in low-power and supply-source-free hardware systems of IoT wireless communication scene.

4 Layout implementation and performance verification

For the implementation of the back-end physical design, the X-axis symmetrical placement for rectifier layout is employed to achieve more balanced current-flowing and thermal distribution, as well as symmetry routing for differential RF signal harvesting. Figure 13 illustrates the complete layout view of the proposed single-stage rectifier circuit, of which the final drawing dimensions excluding the load devices is measured as 76 μm × 70 μm, about 5,320 μm^2.

After running layout parasitic extraction, the rectifier further undergoes post-layout simulation to compare with the pre-layout simulation, in terms of the output voltage level and PCE. Figure 14(a) describes the transient simulation of the output voltage, based on RF signal stimulus of −6 dBm input power and 2.48GHz in frequency. Compared with the average output voltage of 1.05 V in the pre-layout simulation pattern, it only reaches up to 1.03 V in the post-layout pattern.

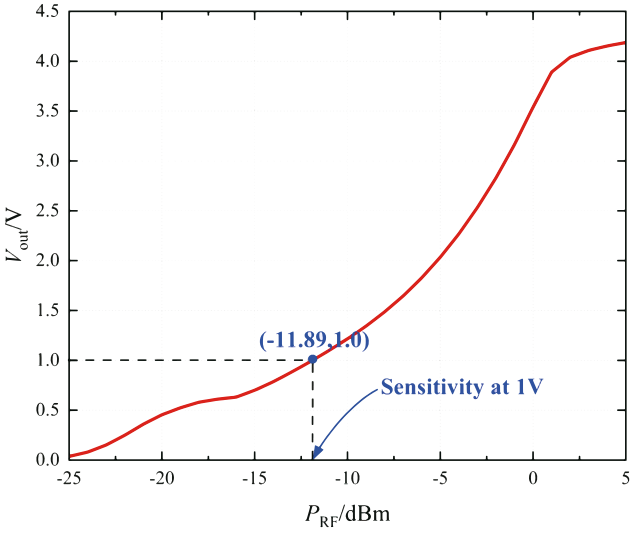

Figure 12: Sensitivity factor measured based on P_{RF}–V_{out} curve with a load resistor of 100 kΩ. Source: Created by the authors.

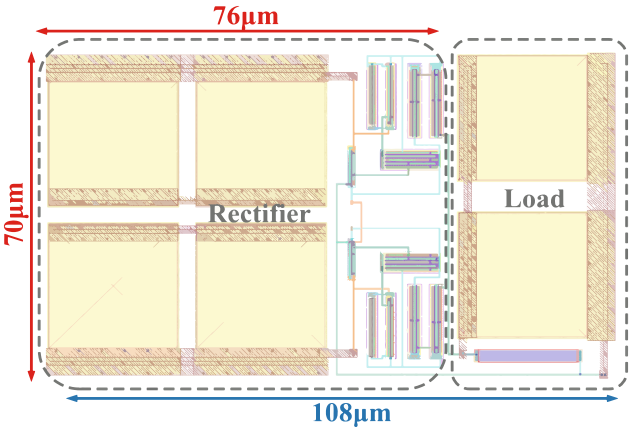

Figure 13: Overall layout view of the differential drive rectifier circuit. Source: Created by the authors.

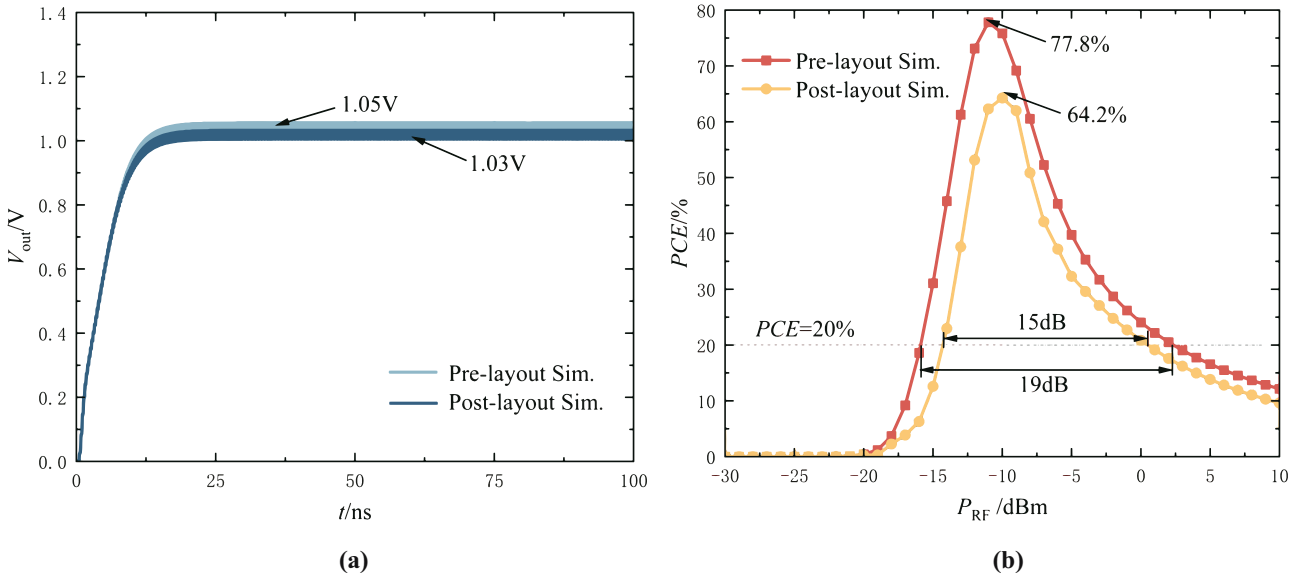

Figure 14: Feature comparison of pre-layout and post-layout simulations: (a) average output voltage level and (b) PCE. Source: Created by the authors.

Moreover, also with the input power of −6 dBm, Figure 14(b) presents the comparison with regard to PCE across various input power level ranging from −30 to 10 dBm. It can be observed clearly that, compared with the pre-layout simulation result, both the PCE and PDR values in post-layout case are decreased regrettably, which are from 77.8% to 64.2% in PCE while 19 dB to almost 15 dB in PDR, respectively. It can be considered the feature of rectifier product would be affected greatly by the energy loss on parasitic RC of MOS transistors and metal interconnection. As can be seen from the simulation results, even the actual physical and parasitic effects are taken into account, the proposed rectifier can still exhibit the excellent performance in PCE and PDR feature, which means that the rectifier is sufficiently robust and practical.

5 Conclusion

This article proposes a micro-sized high-efficiency CMOS CCDDR designed for RF energy harvesting in 2.48 GHz LS-band of IoT communication applications. Focusing on the trouble-shootings of high effective threshold voltage, reverse leakage current, and unstable output voltage conversion in conventional designs, two auxiliary functional modules, termed as DBBA and DFBC, are introduced into the original topology to effectively enhance PCE and widen input PDR. Based on 180 nm/1.8 V RF-CMOS standard technology, the rectifier circuit is implemented as well as the simulation-based performance analysis. The results indicate that the proposed single-stage rectifier circuit can achieve an impressive 77.8% PCE under an input power of −12.5 dBm as a normal signal intensity in 2.48 GHz IoT RF communication. Benefiting from the enhancement of PCE feature, it can be also obtained a stable output supply voltage of 642.46 mV and the higher PDR of 26 dB, meaning the greater dynamic perceiving capability with the sensitivity of −12 dBm at 1 V converted DC output voltage. The final FoM value can be reached up to 54.52 dB as the best one among all the ten comparable design cases. Moreover, by extending the single-stage topology to a double-stage cascade connection, the rectifier can be expected to provide more favorable performance in terms of output voltage, PCE, and PDR. These features on our proposed rectifier are particularly advantageous for realizing source-free and near-zero-energy-consumption hardware operation in LS-band IoT wireless communication systems.

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References

Al-Absi M. A., Alkhalifa I. M., Mohammed A. A., and Al-Khulaifi A. A. (2021). "A CMOS rectifier employing body biasing scheme for RF energy harvesting," IEEE Access, vol. 9, pp. 105606–105611, DOI: https://doi.org/10.1109/ACCESS.2021.3099826.

Alhoshany A. (2022). "A 900 MHz, wide-input range, high-efficiency, differential CMOS rectifier for ambient wireless powering," Sensors, vol. 22, no. 3, DOI: https://doi.org/10.3390/s22030974.

Almansouri A. S., Ouda M. H., and Salama K. N. (2018). "A CMOS RF-to-DC power converter with 86% efficiency and −19.2-dBm sensitivity," IEEE Trans. Microwave Theory Tech., vol. 66, no. 5, pp. 2409–2415, DOI: https://doi.org/10.1109/TMTT.2017.2785251.

Argote-Aguilar J., Wei M.-D., Hutu F. D., Villemaud G., Gautier M., Berder O., and Negra R. (2024). "Wide power range RF energy harvester for powering ultralow-power devices," IEEE Trans. Microw. Theory Tech., vol. 72, pp. 5632–5642, DOI: https://doi.org/10.1109/TMTT.2024.3397389.

Chen H., Cai W., and Chen J. (2021). "Power internet of things technology with energy and information fusion," Power Syst. Protection Control, vol. 49, no. 22, pp. 8–17, DOI: https://doi.org/10.19783/j.cnki.pspc.202163.

Chen H., Liii Z., Chen Y., Chen J., and Wang X. (2020). "Ubiquitous power internet of things based on 5G," Power Syst. Protect. Control, vol. 48, no. 3, pp. 1–8, DOI: https://doi.org/10.19783/j.cnki.pspc.201970.

Chong G., Ramiah H., Yin J., Rajendran J., Mak P.-I., and Martins R. P. (2021). "A wide-PCE-dynamic-range CMOS cross-coupled differential-drive rectifier for ambient RF energy harvesting," IEEE Trans. Circuits Syst. II Express Briefs, vol. 68, no. 6, pp. 1743–1747, DOI: https://doi.org/10.1109/TCSII.2019.2937542.

Choo A., Ramiah H., Churchill K. K. P., Chen Y., Mekhilef S., Mak P.-I., and Martins R. P. (2022). "A reconfigurable CMOS rectifier with 14-dB Power Dynamic Range Achieving >36-dB/mm^2 FoM for RF-based hybrid energy harvesting," IEEE Trans. Very Large Scale Integration Syst., vol. 30, no. 10, pp. 1533–1537, DOI: https://doi.org/10.1109/TVLSI.2022.3189697.

Choo A., Lee Y. C., Ramiah H., Chen Y., Mak P.-I., and Martins R. P. (2023a). "A high-PCE range-extension CMOS rectifier employing advanced topology amalgamation technique for ambient RF energy harvesting," IEEE Trans. Circuits Syst. II Express Briefs, vol. 70, no. 10, pp. 3747–3751, DOI: https://doi.org/10.1109/TCSII.2023.3285977.

Choo A., Ramiah H., Churchill K. K. P., Chen Y., Mekhilef S., Mak P.-I., and Martins R. P. (2023b). "A high-performance dual-topology CMOS rectifier with 19.5-dB power dynamic range for RF-based hybrid energy harvesting," IEEE Trans. Very Large Scale Integration Syst., vol. 31, no. 8, pp. 1253–1257, DOI: https://doi.org/10.1109/TVLSI.2023.3261263.

Chun A. C. C., Ramiah H., and Mekhilef S. (2022). "Wide power dynamic range CMOS RF-DC rectifier for RF energy harvesting system: A review," IEEE Access, vol. 10, pp. 23948–23963, DOI: https://doi.org/10.1109/ACCESS.2022.3155240.

Churchill K. K. P., Ramiah H., Choo A., Chong G., Chen Y., Mak P.-I., and Martins R. P. (2023). "A reconfigurable CMOS stack rectifier with 22.8-dB dynamic range achieving 47.91% peak PCE for IoT/WSN application," IEEE Trans. Very Large Scale Integration Syst., vol. 31, no. 10, pp. 1619–1623, DOI: https://doi.org/10.1109/TVLSI.2023.3299075.

Correia R. and Carvalho N. B. (2016). "Design of high order modulation backscatter wireless sensor for passive IoT solutions," in: 2016 IEEE Wireless Power Transfer Conference (WPTC), pp. 1–3, DOI: https://doi.org/10.1109/WPT.2016.7498833.

Eshaghi M. and Rashidzadeh R. (2020). "An energy harvesting solution for IoT devices in 5G networks." in: 2020 IEEE Canadian Conference on Electrical and Computer Engineering (CCECE), pp. 1–4, DOI: https://doi.org/10.1109/CCECE47787.2020.9255802.

Ijala A. D., Thomas S., and Adetokun B. B. (2022). "The role of energy harvesting in 5G wireless networks connectivity," in: 2022 IEEE Nigeria 4th International Conference on Disruptive Technologies for Sustainable Development (NIGERCON), pp. 1–5, DOI: https://doi.org/10.1109/NIGERCON54645.2022.9803002.

Kim Y.-H., Yoon C., Ahn H.-S., and Lim S.-o. (2019). "Implementation of multi-level modulated-Backscatter communication system using ambient Wi-Fi signal," in: 2019 IEEE International Conference on RFID Technology and Applications (RFID-TA), pp. 476–479, DOI: https://doi.org/10.1109/RFID-TA.2019.8892246.

Kumar M., Kumar S., and Kashyap P. (2021). "Effect of harvesting unpredictability of resources in energy harvesting-WSN," in: 2021 IEEE 4th International Conference on Computing, Power and Communication Technologies (GUCON), pp. 1–5, DOI: https://doi.org/10.1109/GUCON50781.2021.9573729.

Lau W. W. Y., Ho H. W., and Siek L. (2020). "Deep neural network (DNN) optimized design of 2.45 GHz CMOS rectifier with 73.6 peak efficiency for RF energy harvesting," IEEE Trans. Circuits Syst. I Regular Papers, vol. 67, no. 12, pp. 4322–4333, DOI: https://doi.org/10.1109/TCSI.2020.3022280.

Lau W. W. Y. and Siek L. (2017). "2.45GHz wide input range CMOS rectifier for RF energy harvesting," In 2017 IEEE Wireless Power Transfer Conference (WPTC), pp. 1–4, DOI: https://doi.org/10.1109/WPT.2017.7953896.

Lian W. X., Ramiah H., Chong G., Churchill K. K. P., Lai N. S., Chen Y., Mak P.-I., and Martins R. P. (2022). "A 20-dBm sensitivity RF energy-harvesting rectifier front end using a transformer IMN," IEEE Trans. Very Large Scale Integrat. Syst. vol. 30, no. 11, pp. 1808–1812, DOI: https://doi.org/10.1109/TVLSI.2022.3207158.

Lian W. X., Yong J. K., Chong G., Churchill K. K. P., Ramiah H., Chen Y., Mak P.-I., and Martins R. P. (2023). "A reconfigurable hybrid RF front-end rectifier for dynamic PCE enhancement of ambient RF energy harvesting systems," Electronics, vol. 12, no. 1, p. 175, DOI: https://doi.org/10.3390/electronics12010175.

Liu B., Wang P., Li K., Xu B., Zhang J., and Zhang L. (2022). "A precision programmable multilevel voltage output and low-temperature-variation CMOS bandgap reference with area-efficient transistor-array layout," Integration, vol. 87, pp. 74–81, DOI: https://doi.org/10.1016/j.vlsi.2022.06.003.

Liu B., Wang P., Liu X., and Zhang L. (2024). "Response surface methodology based synchronous multi-performance optimization of CMOS low-dropout regulator," Microelectronics J., vol. 143, pp. 106045, DOI: https://doi.org/10.1016/j.mejo.2023.106045.

Liu J., Xiong K., Fan P., and Zhong Z. (2017). "RF energy harvesting wireless powered sensor networks for smart cities,". IEEE Access, vol. 5, pp. 9348–9358, DOI: https://doi.org/10.1109/ACCESS.2017.2703847.

Lu Y., Dai H., Huang M., Law M.-K., Sin S.-W., U Seng-Pan, and Martins R. P. (2017). "A wide input range dual-path CMOS rectifier for RF energy harvesting," IEEE Trans. Circuits Syst. II Express Briefs, vol. 64, no. 2, pp. 166–170, DOI: https://doi.org/10.1109/TCSII.2016.2554778.

Merakeb Y., Huillery J., Bréard A., and Duroc Y. (2022). "Experimental evaluation of the passive RFID technology in pulse wave mode," 2022 3rd URSI Atlantic and Asia Pacific Radio Science Meeting (AT-AP-RASC), pp. 1–3, DOI: https://doi.org/10.23919/AT-AP-RASC54737.2022.9814288.

Moghaddam A. K., Chuah J. H., Ramiah H., Ahmadian J., Mak P.-I., and Martins R. P. (2017). "A 73.9%-efficiency CMOS rectifier using a lower DC feeding (LDCF) self-body-biasing technique for far-field RF energy-harvesting systems," IEEE Trans. Circuits Syst. I Regular Papers, vol. 64, no. 4, pp. 992–1002, DOI: https://doi.org/10.1109/TCSI.2016.2623821.

Moloudian G., Hosseinifard M., Kumar S., Simorangkir R. B. V. B., Buckley J. L., Song C., Fantoni G., and OFlynn B. (2024). "RF energy harvesting techniques for battery-less wireless sensing, industry 4.0, and internet of things: A review," IEEE Sensors J., vol. 24, no. 5, pp. 5732–5745, DOI: https://doi.org/10.1109/JSEN.2024.3352402.

Nagaveni S., Hunasigidad P., Pathak D., and Dutta A. (2024). "On-chip configurable RF energy harvester for biomedical implantable devices," IEEE Trans. Circuits Syst. I Regular Papers, vol. 71, pp. 5030–5039, DOI: https://doi.org/10.1109/TCSI.2024.3416252.

Nagaveni S., Kaddi P., Khandekar A., and Dutta A. (2020). "Resistance compression dual-band differential CMOS RF energy harvester under modulated signal excitation," IEEE Trans. Circuits Syst. I Regular Papers, vol. 67, no. 11, pp. 4053–4062, DOI: https://doi.org/10.1109/TCSI.2020.3006156.

Noghabaei S. M., Radin R. L., Savaria Y., and Sawan M. (2022). "A high-sensitivity wide input-power-range ultra-low-power RF energy harvester for IoT applications," IEEE Trans. Circuits Syst. I Regular Papers, vol. 69, no. 1, pp. 440–451, DOI: https://doi.org/10.1109/TCSI.2021.3099011.

Panigrahi A., Sarania S., and Brahma R. G. (2021). "A low voltage rectifier for Piezo-Electric energy harvesting designed in CMOS technology," 2021 Devices for Integrated Circuit (DevIC), pp. 170–174, DOI: https://doi.org/10.1109/DevIC50843.2021.9455897.

Park J., Kim Y., Cho Y., and Burm J. (2023). "Multi-stage reconfigurable RF-DC converter with deep-n-well biasing using body-isolated MOSFET in 180-nm BCDMOS process," IEEE Trans. Circuits Syst. II Express Briefs, vol. 70, no. 10, pp. 3817–3821, DOI: https://doi.org/10.1109/TCSII.2023.3290178.

Pullwitt S., Tudyka P., and Wolf L. (2022). "Leveraging micro energy sources in energy harvesting wireless sensor networks," in: 2022 17th Wireless On-Demand Network Systems and Services Conference (WONS), pp. 1–8, DOI: https://doi.org/10.23919/WONS54113.2022.9764545.

Ruan T., Chew Z. J., and Zhu M. (2017). "Energy-aware approaches for energy harvesting powered wireless sensor nodes," IEEE Sensors J., vol. 17, no. 7, pp. 2165–2173, DOI: https://doi.org/10.1109/JSEN.2017.2665680.

Sanislav T., Mois G. D., Zeadally S., and Folea S. C. (2021). "Energy harvesting techniques for internet of things (IoT)," IEEE Access, vol. 9, pp. 39530–39549, DOI: https://doi.org/10.1109/ACCESS.2021.3064066.

Schmickl S., Faseth T., and Pretl H. (2020). "An RF-energy harvester and IR-UWB transmitter for ultra-low-power battery-less biosensors," IEEE Trans. Circuits Syst. I Regular Papers, vol. 67, pp. 1459–1468, DOI: https://doi.org/10.1109/TCSI.2020.2970765.

ur Rehman M., Ahmad W., and Khan W. T. (2017). "Highly efficient dual band 2.45/5.85 GHz rectifier for RF energy harvesting applications in ISM band,". In 2017 IEEE Asia Pacific Microwave Conference (APMC), pp. 150–153, DOI: https://doi.org/10.1109/APMC.2017.8251400.

Wong Y., Tan C., Ranjit S., Syafeeza A., and Hamid N. A. (2019). "Energy scavenging for mobile and wireless devices using CMOS rectifier circuit," in: 2019 IEEE International Conference on Industrial Technology (ICIT), pp. 429–433, DOI: https://doi.org/10.1109/ICIT.2019.8755060.

Xu P., Flandre D., and Bol D. (2019). "Analysis, modeling, and design of a 2.45-GHz RF energy harvester for SWIPT IoT smart sensors," IEEE J. Solid-State Circuits, vol. 54, no. 10, 2717–2729, DOI: https://doi.org/10.1109/JSSC.2019.2914581.

Yahya Alkhalaf H., Yazed Ahmad M., and Ramiah H. (2022). "Self-sustainable biomedical devices powered by RF energy: A review," Sensors, vol. 22, no. 17, p. 6317, DOI: https://doi.org/10.3390/s22176371.

Zheng P., Arvind D., and Stanaevi M. (2024). "Design of the dual-channel Dickson rectifier with native NMOS for RF energy harvesting sensors." in: 2024 IEEE International Conference on RFID (RFID), pp. 1–6, DOI: https://doi.org/10.1109/RFID62091.2024.10582673.

Zhu Y., Xu X., Yan Z., and Lu J. (2022). "Prospect of renewable energy integrated distribution network operation in the power internet of things," Power Syst. Protection Control, vol. 50, no. 2, 176–187, DOI: https://doi.org/10.19783/j.cnki.pspc.210317.