

Research Article

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Implementation of cascaded H-bridge DC-link inverter for marine electric propulsion drives

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Abstract: This paper presents a single-phase seven level Cascaded H-Bridge DC-Link (CHBDCL) inverter for marine electric propulsion drives. The speed of propulsion drive can be changed by CHBDCL inverter by converting DC output from the rectifier to variable output voltage with or without change in frequency. The proposed CHBDCL inverter generates more output voltage with minimum harmonic content than classical Multilevel Inverters (MLIs). The CHBDCL inverter necessitates only ' $m + 3$ ' power devices for ' m ' number of levels, although the classical MLIs requires ' $(2m - 1)$ ' power devices. CHBDCL inverter can have the effective performance by utilizing unipolar Sine Pulse Width Modulation (SPWM) and unipolar Space Vector PWM (SVPWM) with sine carrier. The effectiveness of the proposed CHBDCL inverter topology has been verified by using MATLAB/SIMULINK for various modulation indices in terms of voltage levels and harmonic analysis. Furthermore, an experimental setup involving pulse generation from a Field Programmable Gate Array (FPGA) has been used to test the performance of the proposed CHBDCL inverter.

Keywords: cascaded H-bridge DC-link inverter; field programmable gate array; propulsion; sinusoidal reference; space vector reference.

Introduction

In recent years, mechanically coupled ship propulsion systems are progressively being replaced by all electric

propulsion drive systems. The replacement of mechanical couplings with an electrical systems, offers numerous benefits such as increased reliability, enhanced dynamic performance, reduced maintenance cost, more flexibility in ship layout design and reduced fuel consumption. The block diagram of electric propulsion drive system for marine applications is shown in Figure 1. It consists of turbine coupled with generator, phase shifting transformer, rectifier, and power inverter, motor drive applied to propeller and thruster loads. This paper mainly focused on power inverter to improve the power quality of electric propulsion drive for marine applications.

The single line representation of power converter fed electric drive is shown in Figure 2 along with possible improvements and design choices for power converter and electric drive respectively. Power converter is a combination of rectifier integrated with an inverter.

The possible improvements for power inverter to enhance the power quality can be done in two ways mainly: one by using MLIs with less power devices and other by utilizing advanced Pulse Width Modulation (PWM) methods (Naderi et al. 2021; Poorfakhraei, Narimani, and Emadi 2021a; Sunddararaj and Rangarajan 2020). The design choices for an electric drive to attain maximum torque for electric propulsion system can be done by using induction motor and permanent magnet motor drives (Caroline and Beno 2021). Multilevel Inverters (MLIs) are utilized as a favorable elucidation for power quality improvement, to produce high voltage and to attain maximum torque at the propeller shaft in marine electric propulsion drives (Lee and Lee 2021; Poorfakhraei, Narimani, and Emadi 2021a). The existing MLIs are also called as classical MLIs categorized into three types mainly, they are named as Capacitor-Clamped (CC), Diode-Clamped (DC) and Cascaded H-Bridge (CHB) MLIs (Bughneda et al. 2021). These MLIs are consists of more number of devices in terms of power devices or power diodes or capacitors by increasing the number of levels (Hegde, Rao, and Indira 2021; Salem et al. 2020). Therefore, classical MLIs increases cost, control complexity and needs more

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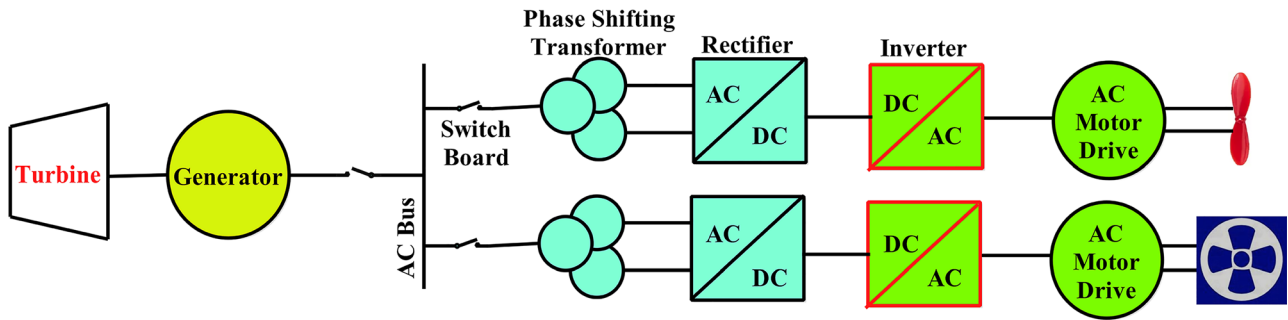


Figure 1: Block diagram of electric propulsion drive system for marine applications.

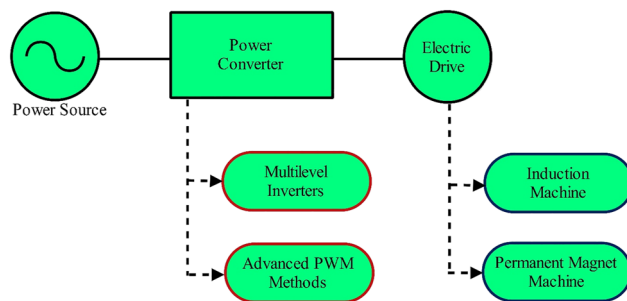


Figure 2: Power converter fed electric drive.

installation area (Vemuganti et al. 2021). To overcome these drawbacks, this paper proposed a CHBDCL inverter with less power devices compared with classical MLIs (Manjunatha et al. 2020). The Cascaded H-Bridge DC-Link (CHBDCL) inverter necessitates only ' $m + 3$ ' power devices for ' m ' number of levels, although the classical MLIs requires ' $2(m - 1)$ ' power devices (Balal et al. 2022; Kubendran, Shuaib, and Roselyn 2022; Rao, Kumar, and Babu 2013). For example, the classical MLIs and CHBDCL inverter requires ten and twelve power devices respectively to generate seven level inverter output (Hassan et al. 2020; Rao, Kumar, and Veerabhadra 2022). Also, this percentage of reduction in power devices still can be increased by increasing number of levels. Using different PWM approaches, the CHBDCL inverter may achieve optimal performance (Easley, Shadmand, and Abu-Rub 2021; Rao, Veerabhadra, and Kumar 2020; Stöttner, Hanzl, and Endisch 2022). In this paper unipolar sine/space vector references with inverted sine carrier modulation techniques are considered for CHBDCL inverter to improve the power quality for marine electric propulsion drives. Finally, prototype model developed for single-phase seven level CHBDCL inverter using Field Programmable Gate Array (FPGA) and validated the simulation results for various modulation indices in terms of voltage levels and harmonic analysis.

CHBDCL inverter configuration

The structure of single-phase seven level CHBDCL inverter is depicted in Figure 3. It consists of a three separate DC sources, 10 power devices and an H-bridge inverter. Table 1 gives a number of parts comparison to generate single-phase seven level output phase voltage across load for the classical MLIs and CHBDCL inverter. The switching table of CHBDCL to generate the single-phase seven levels is given in Table 3. In this structure, DC sources are equal in magnitude i.e., $V_{dc1} = V_{dc}$, where $i = 1, 2$ and 3 .

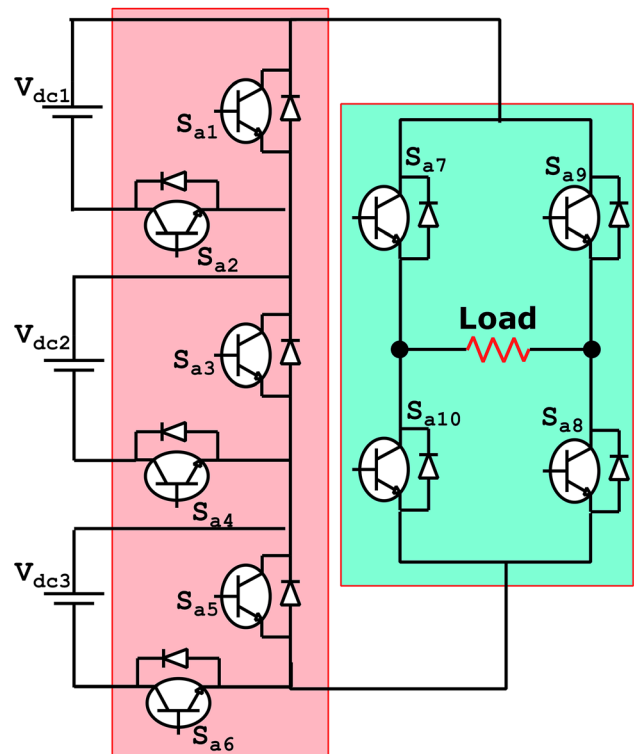


Figure 3: Seven level CHBDCL inverter (single-phase).

Table 1: Component comparison for proposed CHBDCL inverter and existing MLI.

Type of MLI	No. of switches	Clamping diodes/capacitors	DC bus capacitors	DC sources
DC	$2*(m-1)$	$(m-1)*(m-2)$	$(m-1)$	1
CC		$(m-1)*(m-2)/2$	$(m-1)$	1
CHB		–	$(m-1)/2$	$(m-1)/2$
CHBDCL inverter	$(m+3)$	–	–	$(m-1)/2$

The sum of all DC sources equals the maximum value of CHBDCL output voltage, and is given in (1).

$$V_{0,\max} = \sum_{i=1}^s V_{dci} \quad (1)$$

with the help of H-bridge inverter, the positive levels (i.e., 0, $+V_{dc}$, $+2V_{dc}$ and $3V_{dc}$) and negative levels (i.e., $-V_{dc}$, $-2V_{dc}$ and $-3V_{dc}$) are obtained. The seven level stepped output voltage at the load can be obtained using (2) and (3)

$$V_{0,\max} = \sum_{i=1}^n +V_i, \text{ If } S_{a7}, S_{a8} = 1 \quad (2)$$

$$V_{0,\max} = \sum_{i=1}^n -V_i, \text{ If } S_{a9}, S_{a10} = 1 \quad (3)$$

The number of output voltage levels i.e., M_{Levels} of CHBDCL inverter can be obtained by the Equation (4):

$$M_{\text{Levels}} = (2P + 1)Q \quad (4)$$

where 'P' is the number of DC sources and 'Q' is the number of H-bridges.

The number of power devices for the CHBDCL inverter can be assessed by using Equation (5).

$$N_s = 2(P_1 + P_2 + \dots + P_n) + 4Q \quad (5)$$

From Table 2, it is self-evident that as the number of levels in the proposed CHBDCL inverter grows, the number of individual components will naturally decrease.

Figure 4 indicates the variation of power switches for existing MLI's and CHBDCL inverter with respect to number of levels. It can be noticed that the power switches in the proposed CHBDCL inverter drastically reduced when compared to existing MLI's.

PWM scheme

The Sine and Space vector PWM techniques are considered for proposed work. The carrier wave chosen to be a level

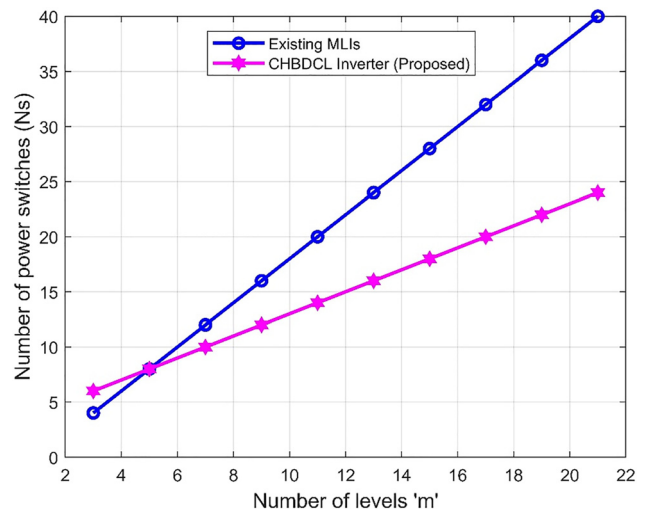
Table 2: Component comparison for proposed CHBDCL inverter and existing MLIs.

Levels	CHBDCL inverter $(m+3)$	Existing MLI $2(m-1)$	% Reduction
7	10	12	16.66
9	12	16	25
11	14	20	30
13	16	24	33.33

Table 3: Switching table of single-phase seven level CHBDCL inverter.

S. no	Cascade phase leg		Single-phase full bridge		Voltage levels
	On switches	Off switches	On switches	Off switches	
1	2, 4, 6	1, 3, 5	7, 8	9, 10	$+3 V_{dc}$
2	1, 4, 6	2, 3, 5	7, 8	9, 10	$+2 V_{dc}$
3	1, 3, 6	2, 4, 5	7, 8	9, 10	$+V_{dc}$
4	1, 3, 5	2, 4, 6	7, 8	9, 10	0
5	1, 3, 6	2, 4, 5	9, 10	7, 8	$-V_{dc}$
6	1, 4, 6	2, 3, 5	9, 10	7, 8	$-2 V_{dc}$
7	2, 4, 6	1, 3, 5	9, 10	7, 8	$-3 V_{dc}$

shifted sinusoid operating at 5 kHz frequency. Figure 5 represents the unipolar sine PWM technique where in a 5 kHz level shifted sinusoid carrier compared with a unipolar sinusoid at 50 Hz. Figure 6 shows the space vector PWM technique, the carrier wave is a sinusoid with 5 kHz like sine PWM but the reference wave is unipolar space vector reference.

**Figure 4:** Variation of power switches with respect to number of levels.

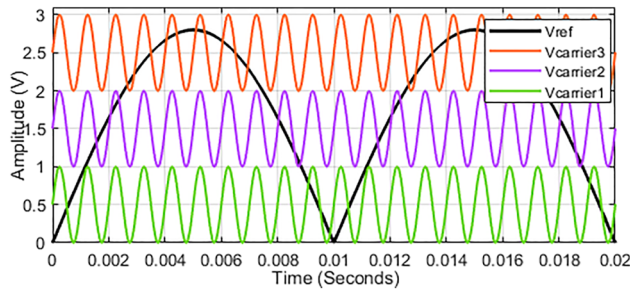


Figure 5: Unipolar SPWM with sine wave carrier.

The range of Modulation index ' M ' for sine reference is varies from 0 to 1 and for space vector reference is varies from 0 to 0.866 (Figure 6).

$$M = \frac{A_r}{\frac{(m-1)}{2} * A_c} \quad (6)$$

where ' m ' denotes the number of levels, ' A_r ' denotes amplitude of reference and ' A_c ' denotes amplitude of carrier.

From Equation (6), the expression for ' M ' to generate seven level waveform is given by Equation (7).

$$M = \frac{A_r}{3 * A_c} \quad (7)$$

Results and discussion of proposed CHBDCL inverter

This section elaborates the simulation and practical outcomes of the proposed CHBDCL inverter for seven level. The Figures 7–15 gives the complete information of the theoretical and practical results obtained for SPWM and SVPWM techniques. The output voltage and the %THD for various modulation indices are compared. The entire results are summarized in the Tables 4 and 5. After careful observation it's evident that the simulation and practical outcomes obtained are in good agreement.

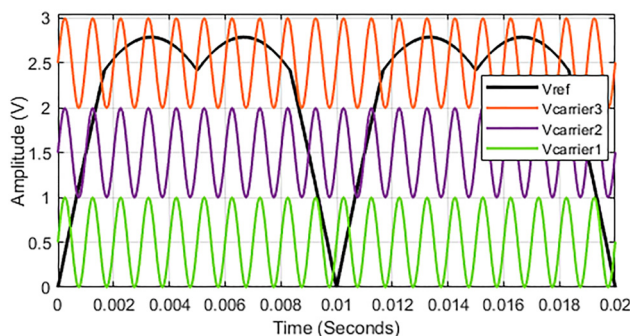


Figure 6: Unipolar SVPWM with sine carrier.v

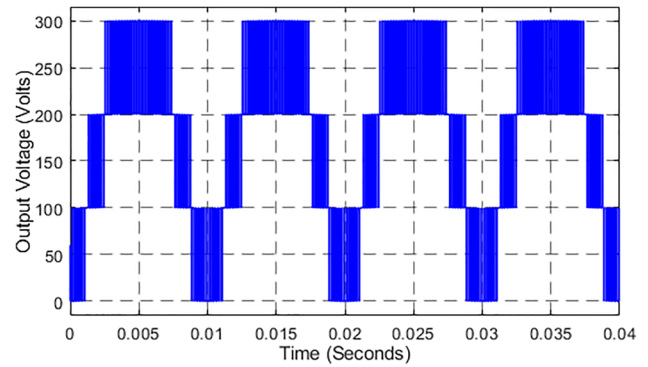


Figure 7: Output voltage for SPWM technique.

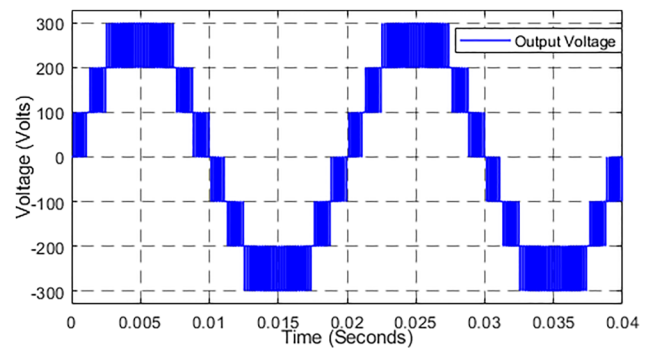


Figure 8: Output voltage for SVPWM technique.

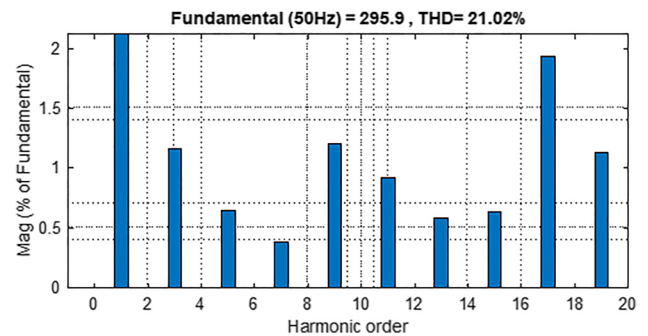


Figure 9: %THD levels for SPWM technique.

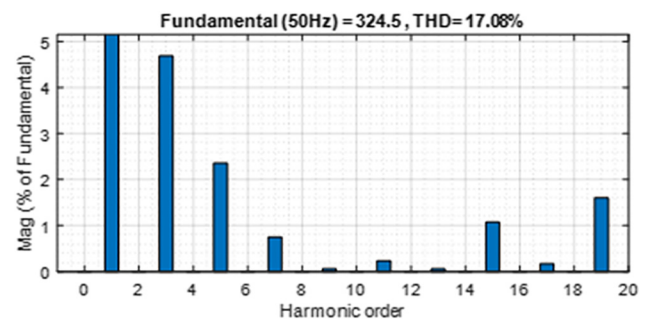


Figure 10: %THD levels for SVPWM technique.

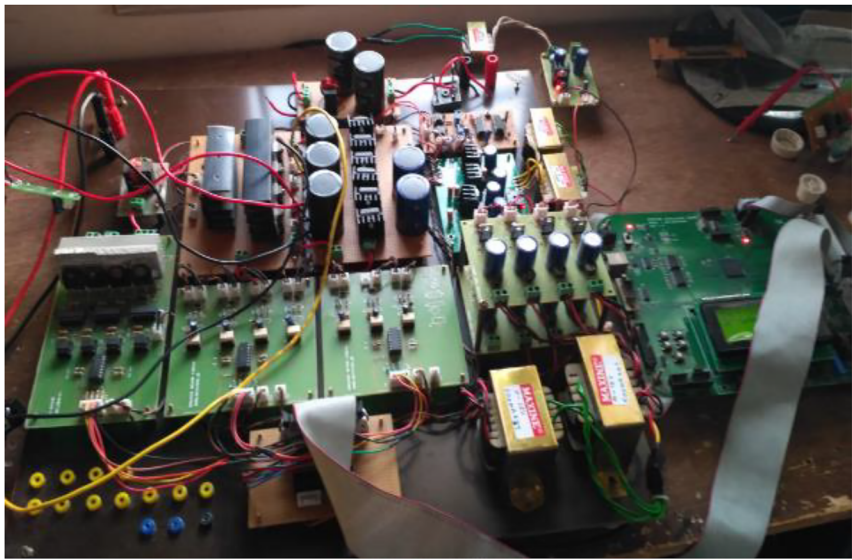


Figure 11: Experimental setup for proposed 7 level CHBDCL inverter.

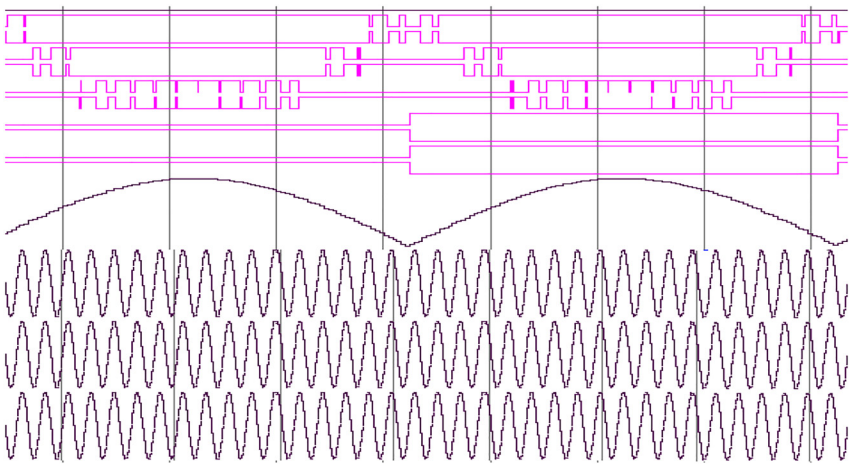


Figure 12: Pulses generated from experimental setup for unipolar SPWM.

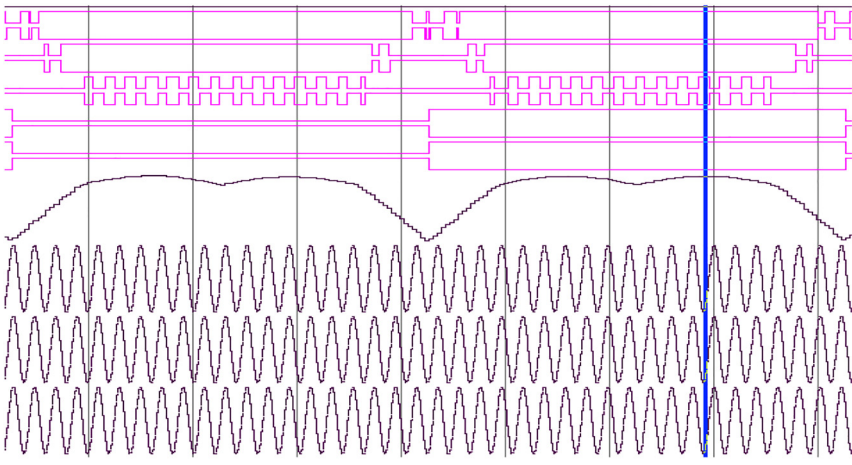


Figure 13: Pulses generated from experimental setup for SVPWM.

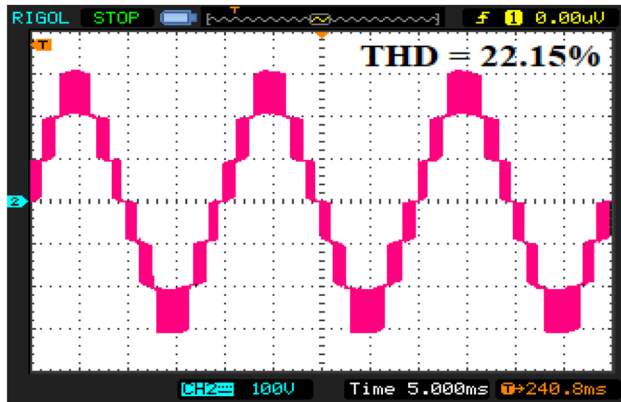


Figure 14: SPWM experimental output voltage with %THD.

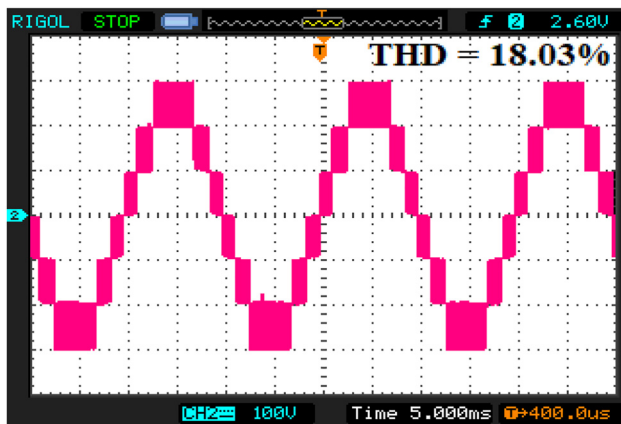


Figure 15: SVPWM experimental output voltage with %THD.

The Tables 4 and 5 gives the comparisons of THD and output voltage levels for different modulation techniques. For a modulation index of 0.9 the SPWM techniques gives simulation and practical THD of 24.57 and 23.48% respectively. Similarly for the same modulation index of 0.9 the SVPWM technique gives simulation and practical THD 19.13 and 18.07% respectively. The output voltages for SPWM and at 0.9 modulation index are 190.1 and 189.2 V respectively in simulation and practical analysis. The output voltages for SVPWM and at 0.9 modulation index are 216.2 and 215.1 V respectively in simulation and practical analysis. So it can be concluded that the SVPWM technique gives better output voltage and low THD levels when compared with SPWM.

Conclusion

In this paper CHBDCL inverter configuration for seven level has been accessed in terms of harmonic analysis by using SPWM and SVPWM approaches. It is concluded that the proposed CHBDCL inverter necessitates only '10' power devices for seven levels, whereas the classical MLIs requires '12' power devices. Furthermore, with increasing levels the required power devices decreases which decreases the hardware complexity. In addition, the proposed CHBDCL inverter requires less installation area and cost-effective. Further, simulation and hardware results of CHBDCL inverter using

Table 4: Comparison of theoretical and experimental output voltage using SPWM and SVPWM techniques for different modulation indices.

S. no	Modulation index	Output levels	RMS voltage using SPWM		RMS voltage using SVPWM	
			Simulation	Experimental	Simulation	Experimental
1	0.5	5	108 V	107.1 V	120.6 V	119.4 V
2	0.6	5	124.8 V	123.7 V	146 V	144.9 V
3	0.7	5	148.9 V	147.5 V	172.9 V	171.6 V
4	0.8	7	171.9 V	170.8 V	193.6 V	192.4 V
5	0.9	7	190.1 V	189.2 V	216.2 V	215.1 V
6	1	7	209.2 V	208.1 V	229.4 V	228.3 V

Table 5: Comparison of theoretical and experimental %THD using SPWM and SVPWM techniques for different modulation indices.

S. no	Modulation index	Output levels	%THD using SPWM		%THD using SVPWM	
			Simulation	Experimental	Simulation	Experimental
1	0.5	5	43.06	42.01	38.91	37.86
2	0.6	5	37.44	36.33	25.87	24.72
3	0.7	5	29.45	28.29	26.58	25.47
4	0.8	7	26.69	25.52	24.09	23.03
5	0.9	7	24.57	23.48	19.13	18.07
6	1	7	21.02	22.15	17.08	18.03

SPWM and SVPWM approaches are included to verify the harmonic analysis. It is concluded that, CHBDCL inverter using SVPWM has given less %THD compared to SPWM. Finally, the simulation results of CHBDCL inverter has been validated with prototype model using FPGA based pulse generation.

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Conflict of interest statement: The authors declare no conflicts of interest regarding this article.

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