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# Power Response of a Planar Thermoelectric Microgenerator Based on Silicon Nanowires at Different Convection Regimes

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**Abstract:** A thermoelectric microgenerator based on multiple silicon nanowire arrays is fabricated and its performance evaluated for different convection regimes. Mature silicon microfabrication technology is used to fabricate the device structure. As a post-process, a bottom-up approach is used to grow silicon nanowires by a VLS-CVD mechanism. The thermal design of the microgenerator features a thermally isolated silicon platform which is connected to the bulk silicon rim through several arrays of silicon nanowires. Simulations are carried out to evaluate the need of an external heat sink to improve the thermal gradient seen by the nanowires and the power output of the microgenerator. Results show a significant improvement with a heat sink raising the thermal gradient from 3 K to approximately 100 K when the external temperature gradient is 300 K. Experimental measurements with different convection regimes also show a radical improvement on the power output comparing natural convection and two different forced convection regimes. The first forced convection regime is a broad airflow from a commercial CPU fan placed on top of the device, while the second (air jet forced convection) uses a syringe to focus the airflow from the compressed air line to the platform. The maximum output power for a natural convection regime is 2.2 nW for a hotplate temperature of 200 °C, while the air jet forced convection regime generates up to 700 nW, which correspond to 35 $\mu W/cm^2$ considering a device footprint of 2 $mm^2$.

**Keywords:** silicon nanowire, thermoelectric microgenerator, energy harvesting, vapor-liquid-solid

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## Introduction

The Trillion Sensor network paradigm requires batch fabrication of energy autonomous sensors. Thermoelectric energy harvesting is a viable alternative to primary batteries as long as residual heat is present. While most of these sensors are fabricated with silicon microtechnology, which allow large volumes of miniaturized sensors at a reduced price, standard thermoelectric modules use exotic elements which are not suitable for microtechnology integration. The lack of good thermoelectric materials in standard silicon technology was assumed before 2008. But nanotechnology allowed silicon to become an active player in thermoelectric energy harvesting. Bulk silicon is known to have a ZT value around 0.01 at 300 K (Weber and Gmelin 1991), but in its nanowire form this value can rise up to 0.6 (Hochbaum et al. 2008; Boukai et al. 2008) changing silicon role from mechanical support to active material.

The idea behind the proposed thermoelectric microgenerator (Dávila et al. 2012) is merging the top-down silicon micromachining technology with the bottom-up silicon nanowire growth (Gadea et al. 2015). On one hand, a thermally isolated silicon platform is fabricated with standard

silicon technology processes including a heater and internal and external current collectors which are electrically isolated where needed through a silicon nitride layer. The platform exposes vertical <111> planes where silicon nanowires would grow laterally reaching the opposite <111> plane on the bulk silicon rim. On the other hand, once the microfabrication is complete, gold nanoparticles are deposited on <111> planes using a galvanic displacement method. These nanoparticles only deposit on silicon exposed walls because all other parts of the device are protected with silicon oxide where nanoparticles do not attach to. Once nanoparticles are deposited, the device is taken to a chemical vapor deposition (CVD) oven where silane is used as a precursor to activate a vapor-liquid-solid (VLS) silicon nanowire growth (Wagner and Ellis 1964). The silicon nanowires grow epitaxially from the place occupied by the gold nanoparticle which acts as a catalyst, until they reach the opposite silicon wall. At that point, nanowires bounce off to a different <111> plane and continue growing until the VLS process is stopped. During the whole process the gold nanoparticles remain at the growing tip of the nanowire. The presented architecture exhibits intermediate silicon trenches between platform and rim running parallel to them. Their purpose is to obtain simultaneously devices with nanowires ensembles of different length using a single VLS-CVD process optimized for 10 µm long nanowires (which is the length between two consecutive trenches)

The main features of the proposed silicon thermoelectric microstructure are that it is a monolithically integrated all-silicon based device which enables batch fabrication using mature silicon microfabrication technology; it presents a planar architecture which facilitates the fabrication of thermally isolated structures which are mechanically robust, resulting in a high yield of successful devices; for technological simplicity, it defines a unileg thermocouple: there is only a P type semiconductor thermoelement and the N thermoelement is replaced by a metal which typically have a Seebeck coefficient two orders of magnitude lower than standard materials used in traditional modules (Rowe 2005). Boron doped silicon nanowires are used as P thermoelement and tungsten is used as the second thermoelement with a Seebeck coefficient of 7.5 µV/K at 300 K (Cusack and Kendall 1958). Finally, the proposed architecture for the single thermoelement is easily scalable to parallel or serial connections of different devices in order to increase the current or voltage, respectively, of the final microgenerator.

## Fabrication

The substrate used is a double side polished silicon on insulator (SOI) wafer with 15 µm thick silicon device layer, 1 µm thick buried silicon oxide, and 500 µm of bulk silicon. The crystallographic orientation of the bulk silicon is a standard <100>, while the one of the silicon device layer is <110>. This is necessary in order to have at least two families of <111> planes perpendicular to the wafer plane, as depicted in Figure 1.

The fabrication process (see Figure 2) starts with a deposition of 300 nm of silicon nitride by LPCVD (Low Pressure Chemical vapor deposition) which acts as an electrical insulator as well as a low thermal conductivity support for electrical connections from the silicon platform to the electrical pads area. The deposited silicon nitride is then patterned to open contact areas close to the nanowires in order to collect electrical current generated by thermal gradients. After that, a local shallow implantation of boron allows to properly dope the

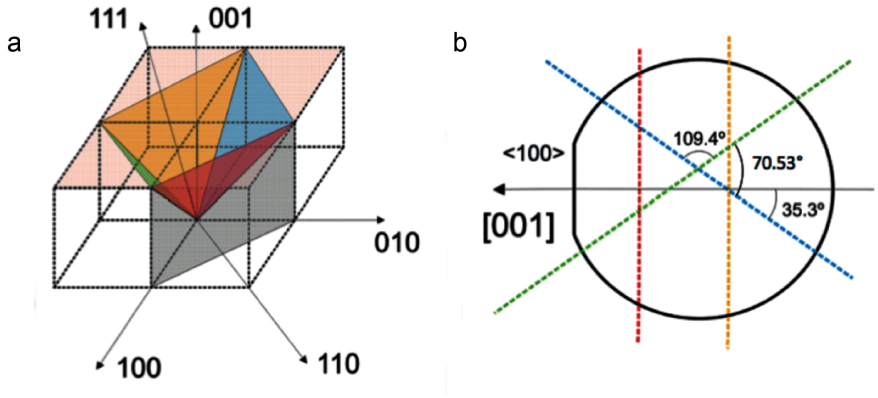


**Figure 1:** Silicon crystallographic planes. (a) Different silicon <111> planes in the standard <100> wafer orientation shown in colours. (b) Silicon <111> planes intersecting with <110> wafer as used in the proposed devices, blue and green planes are perpendicular to the wafer plane (<110>) while red and yellow are oblique planes not used in the final design.

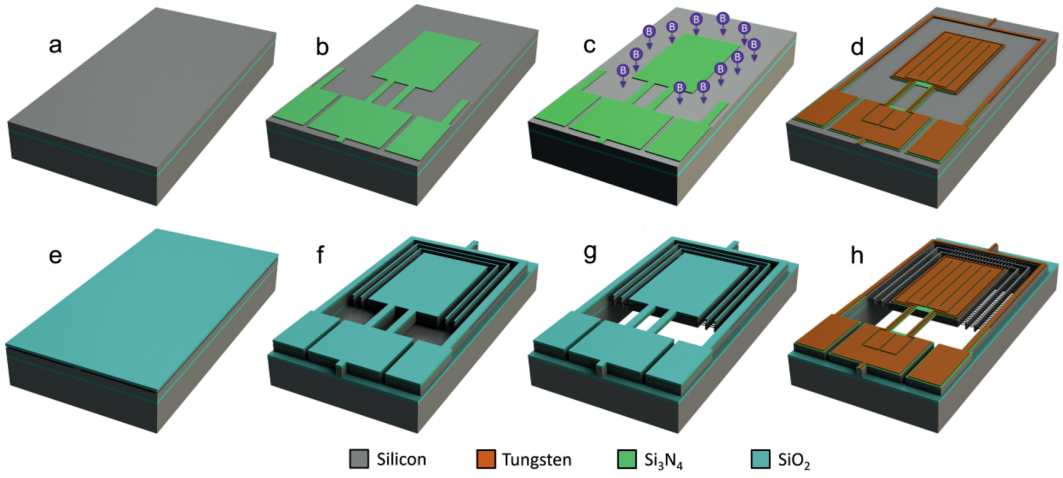


**Figure 2:** Fabrication process steps: (a) double side polished silicon on insulator (SOI) wafer with 15 µm thick silicon device layer (orientation <110>), 1 µm thick buried silicon oxide, and 500 µm of bulk silicon (orientation <100>). (b) LPCVD silicon nitride deposition and patterning. (c) boron doping to improve metal-silicon contact resistance. (d) Metal layer deposition (30 nm thick titanium and 200 nm thick tungsten) and patterning by lift-off. (e) Deposition of a thick silicon oxide to passivate the device. (f) RIE of silicon oxide and silicon nitride layer and DRIE of silicon device layer patterning silicon platform and trenches exposing <111> planes. (g) Bottom side DRIE of silicon to release the platform, KOH etch of the silicon under the silicon nitride supports, galvanic displacement to deposit gold nanoparticles on exposed silicon <111> planes, and VLS-CVD growth of silicon nanowires. (h) Final passivation removal and CPD to obtain ready to test devices.

exposed silicon (silicon nitride acts as a mask to the implantation) resulting in highly doped silicon areas where the metal is to be deposited, improving the contact resistance between metal and silicon and avoiding any electrically rectifying behaviour. Then, the metal is deposited and patterned by lift-off. A 30 nm thick layer of titanium and a 200 nm thick layer of tungsten are used as metal layers. The titanium plays a double role, improving the adhesion of the tungsten layer to silicon, and reducing the electrical contact resistance due to the formation of titanium silicide in the interface. To activate this formation a rapid thermal annealing (RTA) process is done at 700 °C for 30 s with heating ramps of 150 °C/s in vacuum. Once the silicon nitride and metal are defined, LPCVD silicon oxide is used to passivate all exposed layers to prepare for the silicon micromachining steps on top and bottom wafer sides. Then a photolithography step is used to define the geometry of the platform and the trenches between the platform and the surrounding rim, followed by a dry etch of the passivation (silicon oxide) and silicon nitride, which exposes the silicon device layer we want to remove. A second dry etch process (deep reactive ion etching (DRIE)) is done to eliminate the silicon and finally exposing the buried silicon oxide (BOX) layer of the SOI wafer. A proper DRIE recipe is used so that unwanted notching effects are reduced once the silicon oxide is reached. This completes the top side processing of the SOI wafer. A double side aligned photolithography and DRIE on the bottom side is done to remove the silicon bulk under the platform, trenches and silicon nitride supports. This DRIE stops once it reaches the BOX layer (1 µm thick), which is later removed by vapour HF from the bottom side. After that the wafer is diced into 7 mm × 7 mm chips and further processed. Each chip contain several devices. Despite all subsequent processes can be done at wafer level, processing chips is easier and more tests can be done to improve the yield and performance of final devices at this early stage of prototyping. Once diced, the chips are immersed in a 40 % KOH solution at 80 °C for 10–20 min to etch the silicon beneath the silicon nitride supports, thus reducing the thermal leak paths between silicon platform and rim. The platform, rim, and the connecting supports hosting the metal tracks are designed in such a way that vertical walls of platform and rim follow <111> planes, while the ones defined by the supports follow non-<111> planes. Therefore, once exposed to KOH only these planes are laterally etched and the platform and rim (and intermediate trenches) do not suffer any modification during the release of silicon nitride supports. This significantly decreases the supports thermal conductance, and thus the platform is much better isolated. As a final step, gold nanoparticles are attached to silicon exposed surfaces by a galvanic displacement method and once deposited, silicon nanowires are grown on a CVD by the VLS mechanism using silane as a precursor and diborane for boron doping of silicon nanowires. Once silicon nanowires are grown on the device, the remaining passivation

is etched with 5 % HF, a critical point drying (CPD) process is used to avoid the silicon nitride supports collapsing under the surface tension stress of ambient drying, and ready to test devices are obtained.

One of the most critical steps in the whole process is the KOH step to etch the silicon beneath the silicon nitride supports and polish the already exposed <111> planes reducing the scalloping after the DRIE. The whole structure layout has been designed in order to expose <111> planes on silicon with concave corners. This way the anisotropic etch does not progress significantly as opposed to convex corners which expose higher order planes which are etched and end up etching also the exposed <111> planes. The images shown in Figure 2 are a schematic representation of the final designs shown in Figure 3. These SEM images show the designed device, without nanowires, featuring multiple trenches, internal and external collectors, and integrated heater and temperature sensor. The temperature sensor is used to have a reliable temperaure measurement of the top silicon temperature outside the platform. The integrated heater itself can be used simultaneously as a heater and as a temperature sensor. All readings of these temperature sensors are done using a four-point measurement to neglect contact resistance of the probe (or wire bonding in case of packaged devices). To correlate resistance measurements with temperature readings, the metal temperature coefficient of resistance (TCR) has been previously measured in the range of ambient temperature to 250 °C for each device individually. On the right image of Figure 3 the opened trenches are shown as perfectly flat <111> silicon planes after the KOH step and that the structures do not suffer from prolonged etching due to slow etch rate of <111> planes in concave corners. The thermally isolated platform has a size of $1{,}000 \times 1{,}000\,\mu m^2$. Although the SEM image on the left can be thought of as being tilted, it is actually a top view image. The angles seen correspond to 109.4° or 70.53° depending on the corner (see Figure 1, right), and obey to the alignment to <111> vertical planes as commented before.

## Modelling and Simulation

In order to optimize the power output of the thermoelectric microgenerator, the thermal gradient seen by the nanowires needs to be as close as possible to the external thermal gradient which is the temperature difference between the hot surface and the ambient temperature. To achieve that, the silicon nanowires thermal resistance needs to be increased while the thermal resistance from the platform to the ambient needs to be as low as possible. The authors already reported (Dávila et al. 2012) a first generation device generating $9\,\mu W/cm^2$ when the device was placed on top of a hotplate at 300 °C under a given forced convection condition. But the thermal gradient seen by the nanowires was only 27 °C. In fact, if the integrated heater on the platform was used to heat the platform itself at 300 °C above ambient temperature, the power density became $1.44\,mW/cm^2$. Since those results were published, several changes have been applied to the design of the thermoelectric microgenerator (Fonseca et al. 2015) to maximize the power output.

Although these design changes improve the platform thermal isolation from the silicon bulk, the platform is still poorly connected with the ambient. The only cooling mechanism available for the platform is natural convection (radiation is neglected for the temperatures

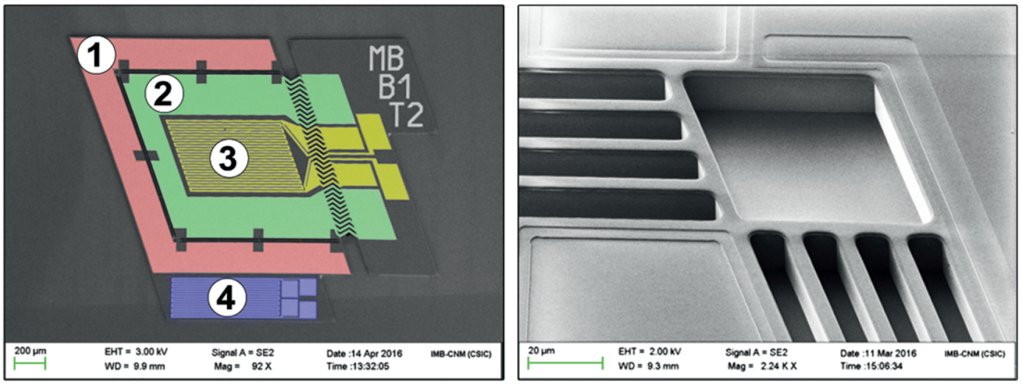


**Figure 3:** SEM images of a final device before silicon nanowire growth. Left image shows a two trench design, with 100 µm long zig-zag silicon nitride supports. Four main elements can be identified: U-shaped external collector (1), U-shaped internal collector (2), integrated meandering heater for test and characterization purposes with four-point measurement capabilities (3), external temperature sensor (4). Right image shows a detail of a platform corner for a four trench device. Each trench has a 10 µm gap and the silicon bars are 6 µm wide.

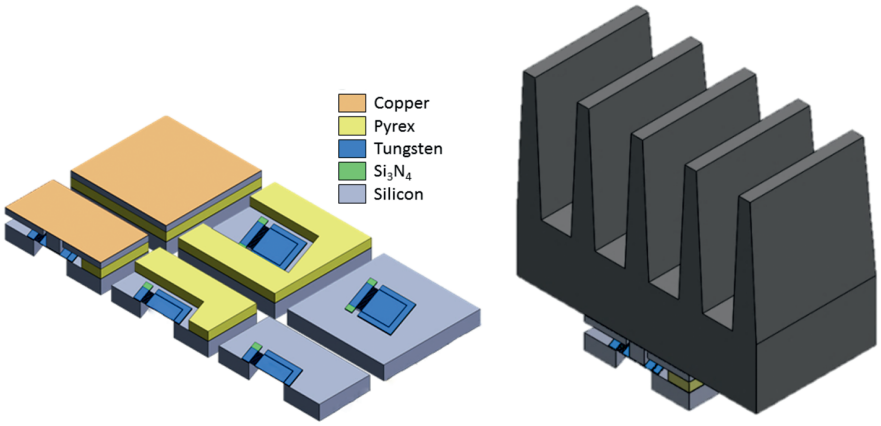


**Figure 4:** Model used to evaluate the temperature distribution of the thermoelectric microgenerator with a heat sink placed on top of the device. A Pyrex spacer is used to place a silicon adapter (with a deposited copper thin film) on top of the device to properly contact the silicon platform with a silicon column.

considered), which is quite low due to the small footprint of the platform (roughly 1 $mm^2$). Heat sinks are a common solution to improve heat dissipation by convection. A finite element model in COMSOL is evaluated for the current design of the thermoelectric microgenerator with a heat sink (7 mm × 7 mm) placed on top of the device as is shown in Figure 4.

The boundary conditions applied to the model are setting the bottom temperature to 600 K and natural boundary conditions to an ambient temperature of 300 K on the exposed surfaces. The results for such conditions are shown in Figure 5, where in one case (left image) the heat sink has been removed. Both temperature distributions are shown with the same scale to highlight the significant role of the heat sink. Nevertheless, the temperature span for the case without a heat sink is roughly 2–3 K of the maximum external temperature gradient (300 K), whereas with a heat sink this value reaches almost 100 K.

## Experimental Methods

The thermoelectric microgenerator provides an output power in response to a thermal gradient between the silicon bulk rim and the thermally isolated platform. This thermal gradient can be internally generated through the integrated heater on the platform or externally generated by placing the thermoelectric microgenerator on a hot (or cold) surface and use the ambient temperature to cool (or heat) the platform. The former case is called *test mode* and the latter case *harvesting mode* (see Figure 6). In the so-called *test mode*, the voltage and current supplied to the integrated heater are continuously monitored to compute the total dissipated power as well as the mean temperature of the platform through the previously calibrated TCR and the calculated resistance. In addition, due to the high thermal conductivity of silicon, the whole silicon bulk is near to ambient temperature as can be validated through an external temperature sensor (blue serpentine placed close to the U-shaped external collector in Figure 3). The thermal gradient seen by the silicon nanowires can be calculated with these two temperature measurements.

To obtain these measurements a couple of sourcemeters (Keithley) and a Linkam station with a thermal chuck, capable of reaching up to 350 °C, are controlled with LabVIEW. The TCR measurement takes place in an oven which is heated up to 250 °C and then it is slowly cooled down while temperature is read from a thermocouple and four-point resistance measurements are taken every few seconds until the temperature reaches 30 °C.

## Results

After seeing the preliminary studies on device performances, and while a heat sink adapter is being designed, fabricated and integrated on the final device, different convection regimes were tested on available devices to evaluate the maximum performance in harvesting mode operation. To that end, a natural convection and two forced convection regimes were tested on 3 different devices with 1, 3 and 6 trenches. The first forced convection regime is a standard CPU fan on top of the device (see Figure 7) while the second forced convection regime

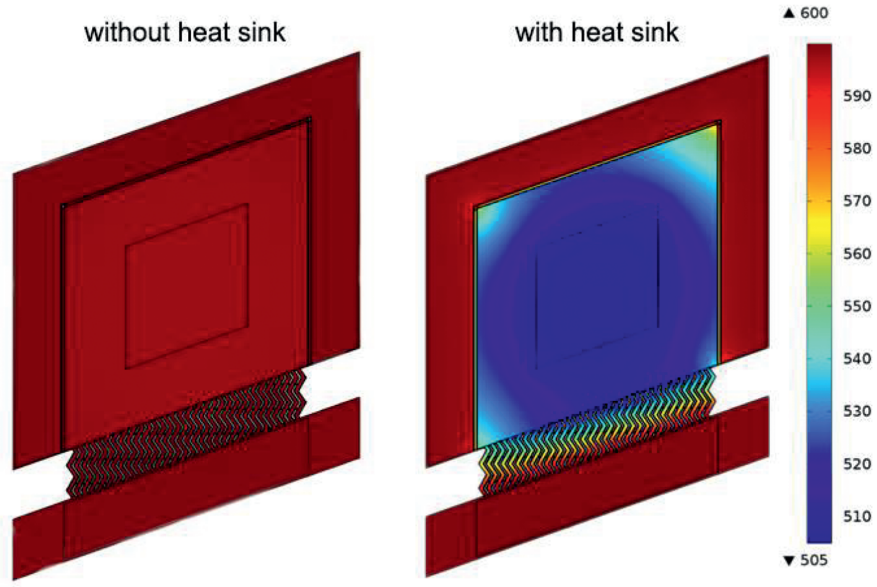


**Figure 5:** Temperature distribution from finite element model with and without a heat sink. The device bottom temperature is fixed at 600 K while the top surfaces have a natural convection to an ambient temperature of 300 K. Both models are plotted with the same temperature range to highlight the differences. The temperature span without a heat sink is only 3 K, while with a heat sink it reaches almost 100 K.

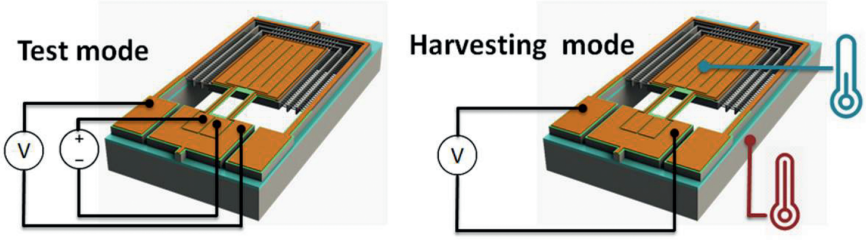


**Figure 6:** Thermoelectric microgenerator operation modes, (left) test mode using the integrated heater to generate the thermal gradient, and (right) harvesting mode using thermal gradients present in the ambient.

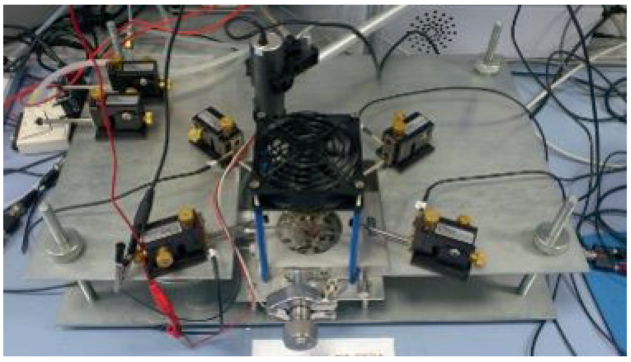

**Figure 7:** Forced convection setup with a standard CPU fan on top of the Linkam chamber.

(air jet convection) is assembled using a syringe connected to compressed air in the laboratory and aimed vertically towards the platform being measured.

Figure 8 shows the results of this study where different convection regimes are applied to different thermoelectric microgenerators. All of them are measured under harvesting mode and placed on top of a hotplate at different temperatures from 50 °C to 200 °C in steps of 25 °C. Three different devices are measured under these conditions with 1, 3 and 6 and trenches. Each trench has a gap of 10 µm, therefore the total trench length for each device is 10 µm, 30 µm and 60 µm respectively. After the jet forced convection measurement, the single trench device broke and further measurements were only carried out on 3 and 6 trench devices. It can be seen that the power output for natural convection is in the order of 1 nW even for 200 °C hot plate temperature. It is worth mentioning that the x-axis in Figure 8 is the temperature measured by a external temperature sensor of each device. We noted that the surface temperature is very sensitive to the attachment

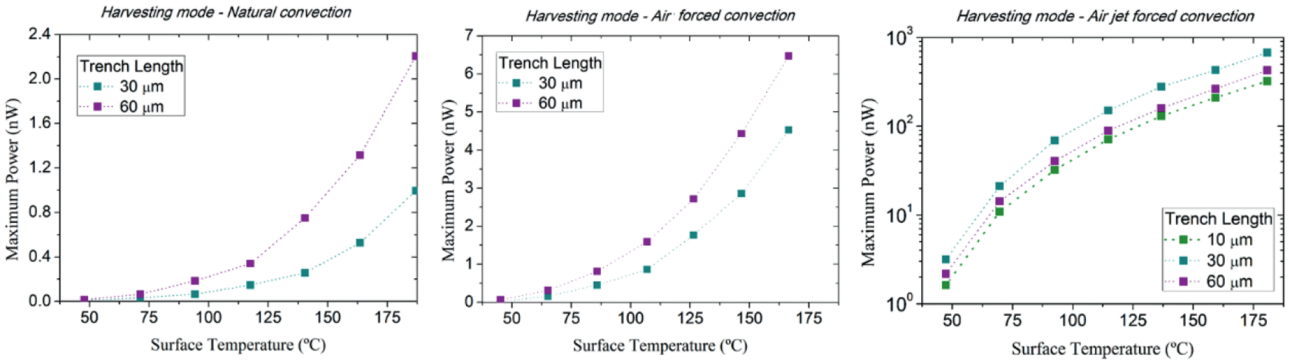


**Figure 8:** Thermoelectric microgenerator power output for different trench lengths under different convection regimes in harvesting mode. They are plot versus the surface temperature of each device measured by the external temperature sensor. The hot plate temperatures applied range from 50 °C to 200 °C in steps of 25 °C.

setup used to place the device on top of the linkam thermal chuck. In addition, in forced convection conditions this temperature difference, between the hot plate and the top device surface, increases due to a larger cooling rate not only of the silicon platform but also of the top surface of the silicon rim. This effect is reduced in the jet forced convection because with the syringe we are able to better confine the air flow on top of the platform and not on the surrounding surfaces.

As we already know, natural convection for a small footprint area poses a really high thermal resistance to ambient which translates into low thermal gradients across the silicon nanowires. On the other hand, after switching on the CPU fan, and changing the convection regime to a forced convection one, the power output improves by a factor of approximately three. When the jet forced convection regime is measured, the power output reaches almost 0.7 μW for a hot plate temperature of 200 °C.

It can be observed that for both natural convection and fan forced convection, the better performance corresponds to the device with longest nanowires. On the other hand, in the air jet forced convection regime, the detrimental effect of higher electrical resistance of longer nanowires outperforms the benefit of their larger thermal resistance because the thermal resistance of the platform to the ambient already assures a significant ΔT. This trade-off makes the 30 μm long nanowire device perform better in terms of power output than 10 μm devices (low thermal gradient) and 60 μm devices (large electrical resistance).

## Conclusions and Further Work

The design, fabrication and characterization of a silicon nanowire based thermoelectric microgenerator are presented. The device, featuring multiple 10 μm trenches, has been designed to expose the appropriate <111> silicon planes for a subsequent silicon nanowire bottom-up growth process in active silicon areas. A thermally isolated platform is responsible for generating the appropriate thermal gradient across the nanowires. Simulations confirm the need for a heat sink integrated on the thermally isolated platform to reduce the thermal resistance from the platform to the ambient. Results show that when an external temperature gradient of 300 K is present, the temperature gradient seen by the silicon nanowires is below 3 K without a heat sink, and around 100 K with a heat sink. Moreover, different devices have been measured obtaining a power output of 2.2 nW, 6.5 nW and 0.7 μW (11 nW/cm$^2$, 32.5 nW/cm$^2$ and 35 μW/cm$^2$, if considering a device footprint of 2 mm$^2$), for natural convection, fan forced convection and air jet forced convection conditions, respectively. Experiments show that although longer nanowires exhibit higher thermal resistances leading to larger temperature differences (and higher voltages), their higher electrical resistance comes into play and less power is obtained when the thermal resistance of the platform towards the environment is already made low enough by certain forced convection conditions (or presumably by an effective heat sink). The heat sink adapter and its integration on the thermoelectric microgenerator is currently being developed.

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