Research Article

Yuan Rao*, Kelly M. McEachern, and David P. Arnold

A Compact Human-Powered Energy Harvesting System

Abstract: A fully functional, self-sufficient body-worn energy harvesting system is presented in this paper. The system is designed for passively capturing energy from human motion, with the long-term vision of supplying power to portable, wearable, or even implanted electronic devices. Compared with state-of-the-art vibrational systems, the system requires no external power supplies and can bootstrap from zero-state-of-charge to generate electrical energy from walking, jogging, and cycling; convert the induced AC voltage to DC voltage; and then boost and regulate the DC voltage to charge a Li-ion-polymer battery. Measurements show that at open-load the system turns on when the input is above 1 V_{pk} and turns off when the input drops below about 600 mV_{pk} with no measurable standby power consumption. Tested under normal human activities (walking, jogging, and cycling) when worn on different parts oze body, the 70 cm^3 system is shown to charge a 3.7 V rechargeable battery at charge rates ranging from 33 μW to 234 μW.

Keywords: energy harvesting system, interface circuit, magnetic energy harvester, rechargeable battery, human movement

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Introduction

Vibrational energy harvesting systems that convert ambient mechanical energy in the environment to usable electrical energy represent a promising emerging technology to achieve autonomous, self-renewable, and maintenance-free operation of wireless electronic devices. As depicted in Figure 1, a complete energy harvesting system comprises three main components: a transducer that converts ambient energy into electrical energy, an interface circuit that conditions and regulates the energy, and a load that absorbs the energy. The transducer converts the energy from a source domain (mechanical, solar, thermal, etc.) to the electrical domain. In the case of vibrational or motional energy conversion, the transducer is commonly called an "energy harvester." The interface circuit serves to extract a maximum amount of energy from the transducer and make the energy usable to the load. This may include voltage rectification, voltage regulation, and other power management functions. The load may comprise power consuming electronic devices (circuits, sensors, actuators, etc.) and/or energy storage elements (batteries, capacitors, super capacitors and etc.).

There has been a significant increase in the research on devices and circuits for harvesting vibrational energy in recent years (Meninger et al. 2001; Pereyma 2007; Beeby, Tudor, and White 2006; Roundy, Wright, and Rabaey 2003; Starner and Paradiso 2004). A majority of efforts have explored harvesting from vibrating structures (machinery, cars, buildings, etc.), with much fewer exploring harvesting mechanical energy from human-induced vibrations. Additionally, most interface circuits designed for vibrational energy harvesting are powered either by an external power supply or by the circuit output (Szarka, Stark, and Burrow February 2012; Chao 2011; Peters, Ortmanns, and Manoli 2007; Le et al. 2006; Peters et al. 2008; 2010; Lam, Ki, and Tsui 2006; Cheng et al. 2009; Anton, Erturk, and Inman 2009; Mendez-Delgado and G. Serrano 2010). When used in complete vibrational energy harvesting systems, standby power of the interface circuits may drain the energy storage element and cause a startup problem after if there is a long idle time interval between two harvesting cycles.

To solve this problem, in this paper, an "input-powered" interface circuit architecture is developed to power the active electronics using the unconditioned input AC voltage waveforms. Compared with state-of-the-art vibrational energy harvesting circuits, the input-powered

Part of the content has been published in the PowerMEMS 2013 Conference.

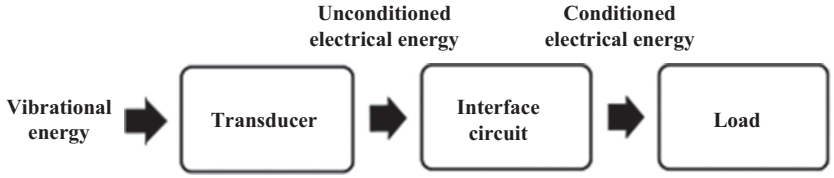


Figure 1 Block diagram of an energy harvesting system

interface circuit achieves zero standby power while maintaining reasonable efficiency. A shortcoming of the input-powered design, however, is the comparatively higher minimum input voltage for operation of the circuit, which arises due to the required rail-to-rail voltage of the circuit.

Using the input-powered interface circuit, a fully self-contained energy harvesting system is demonstrated. In the system, a non-resonant electrodynamic harvester designed specifically for harvesting energy from human movements. "System design" section details the design of the harvester, interface circuit, and storage elements and their integration into a fully functional system prototype. In "Experimental results" section, the interface circuit is first bench-top characterized, and then the complete harvester system prototype is characterized when worn by a person during normal human movements, including walking, running, and cycling. "Conclusions" section presents conclusions from the work.

System design

The design of an energy harvesting system is very different than the design of a traditional battery-powered system. Whereas battery-powered systems are typically limited by energy, energy harvesting systems are typically limited by power (energy is theoretically limitless). Thus, maximizing the output power is the main goal of an energy harvesting system. Since there is typically no "cost" or "penalty" for the input mechanical energy, the mechanical-to-electrical efficiency is not the primary concern. The output power, however, is dependent on the size and power density of the energy harvesting transducer and the efficiency of the associated interface circuitry, both of which should be optimized simultaneously.

Moreover, to design a high-performing energy harvesting system, all function blocks should be considered together as one cooperative system, because the performance degradation of any one component or any incompatibility of one component with another will make the system less efficient. Sometimes the improvement of one component may come with a performance loss elsewhere. For example, the interface circuit would benefit from higher input voltage and power for larger output power and higher efficiency. However, to generate higher voltage and power, the transducer size might need to become larger, and the power density of the whole system may be sacrificed.

Energy harvester

Compared with mechanical vibration sources, human-induced motions are challenging for energy harvesting design because of their low-frequency (1–10 Hz), aperiodic, and time-varying characteristics. The commonly used high-Q resonant-type energy harvesters, which are based on an under-damped, single-degree-of-freedom, mass-spring-damper system are generally not well suited for human movement energy harvesting. The reason is that these resonant systems are optimized to achieve maximum output power within a small-frequency range under oscillatory accelerations. Moreover, it is difficult to tune the resonant frequency to the low frequencies of human motions (1–10 Hz) and maintain high quality factor, especially all while maintaining compact device dimensions. Another major restriction of conventional resonant harvesters is that they are typically designed for only one rectilinear degree of freedom, while normal human movements occur in three dimensions and involve a high degree of rotational, rather than oscillatory, motions.

The above challenges motivate the use of a non-resonant harvester architecture, which can respond over a broad range of vibration frequencies and amplitudes, and the use of a multi-directional architecture that can respond to motions in multiple axes. Our research group has previously reported a unique, omnidirectional electrodynamic energy harvester design (Bowers and Arnold 2009), which is replicated with modifications in the system reported here.

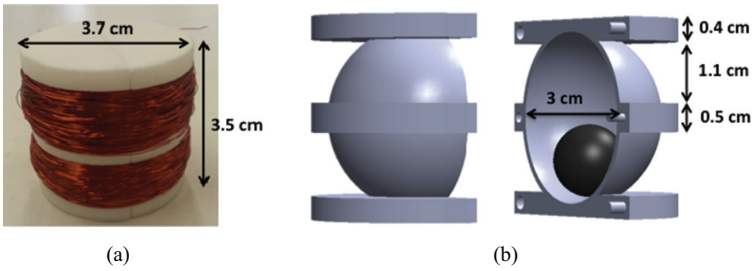


Figure 2 Non-resonant, omnidirectional electrodynamic energy harvester: (a) photograph and (b) 3D schematic

As shown in Figure 2, the harvester structure is fabricated in two symmetric hemispheres using a Nylon plastic material from a 3D printer (Shapeways, Inc. NY, USA). The two halves are fit together to form a spherical cavity (diameter = 3 cm) with a permanent magnet ball (diameter = 1.27 cm, Grade N40 NdFeB) inside. The upper and lower coil bobbins are then each wrapped with ~1,400 turns of 34 AWG copper wire forming two independent coils with a resistance of 110 Ω each. The harvester has a total volume of about 39 cm^3 and weighs 68 g.

In operation, the magnet ball moves chaotically within this spherical housing when subjected to external vibrations/motions. The motion of the magnet ball induces a time-varying magnetic flux in each of the surrounding coils, thus generating a voltage according to Faraday's Law. When an electrical load is connected, a current will flow through the coil, thus converting mechanical energy into electrical energy. In the experiments, the two coils are counter-wound and connected in series to improve power generation.

Energy harvesting interface circuit

The block diagram of the interface circuit is shown in Figure 3, where the energy harvester is represented by a voltage source V_S and an output impedance of R_S. The interface circuit consists of an AC/DC stage and a DC/DC stage, converting the pseudo-random voltage from the harvester to charge the load. The DC/DC stage is a boost converter with on-chip DC/DC controller to provide a regulated output voltage for battery charging.

The entire interface circuit is input-powered by the time-varying voltage supplied from the harvester. The AC/DC converters in the AC/DC stage are powered by their AC input in a straightforward way. The DC/DC stage may not first appear input-powered, because V_A, instead of the DC input V_P, supplies the DC/DC controller in this stage. However it is still an input-powered converter, considering that the power of V_A is also from the input-side voltage source (V_S).

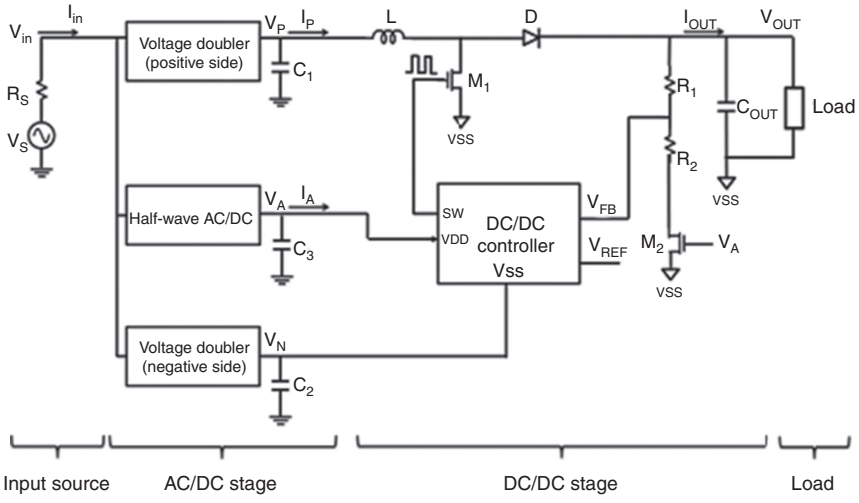


Figure 3 Block diagram of the interface circuit

AC/DC stage

Two different AC/DC converters are used in the AC/DC stage. The first is a voltage doubling AC/DC converter (often called voltage doubler), which serves as the primary rectifier in the power path. The second is an auxiliary half-wave AC/DC converter, which is used to provide a more stable supply voltage for the DC/DC converter stage.

The positive side of the voltage doubler converts the AC input to a positive DC voltage (V_P), which is then regulated by the DC/DC stage. The negative-side voltage doubler generates a negative DC voltage, which is connected to the ground (VSS) of the DC/DC stage. Therefore, the voltage difference between the dual outputs of the voltage doubler is the actual DC input seen by the DC/DC converter. Compared with the previous interface circuit design, which used a half-wave rectifier architecture (Roundy, Wright, and Rabaey 2003), the voltage doubler front-end used here has the benefit of higher output power, and also lower voltage conversion burden to the following DC/DC stage.

Voltage doubling AC/DC converter

There are several reasons why the voltage doubling AC/DC converter is chosen for the main signal path other than full-wave and half-wave topologies. First, the single-diode rectification used in each side of voltage doubler offers improved low-power efficiency than the four-diode full-wave rectifier, especially when the diode forward voltage drop is comparable with the input amplitude (Clare and Burrow 2010). Second, in vibrational energy harvesting systems, the input AC voltage is often much lower than the desired output DC voltage on the load, and therefore the voltage doubling effect of voltage doubler can reduce the voltage amplification burden of a subsequent step-up converter. Another important benefit is the reduced circuit complexity and power loss associated with the fewer number of diodes compared with full-wave topology, particularly if active diodes are used.

Figure 4 shows the voltage doubler circuit. It consists of two half-wave rectifiers: positive-side rectifier and negative-side rectifier. Each side of the circuit operates on the opposite half-cycle of the input waveform. The load (R_{LOAD}) is connected across the positive and negative output terminals. So the final DC output is the difference between the positive-side DC output (V_{OUT+}) and the negative-side DC output (V_{OUT-}), which is twice of the AC input amplitude (V_{IN}) in the ideal case.

The rectifiers use active-diode topologies to reduce the voltage drop in comparison with conventional

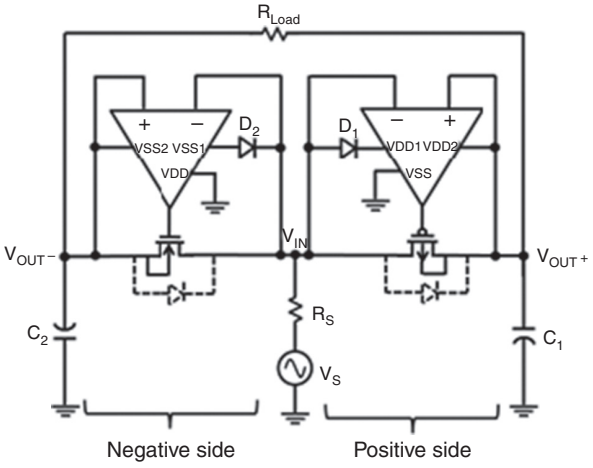


Figure 4 Voltage doubler based on active diodes

junction-diode rectifiers. The active diode comprises a comparator and a MOSFET switch. The two terminals of the switch are equivalent to the anode and cathode terminals of a diode. The comparator detects the voltage difference between these two terminals and determines when to turn on or off the switch. A PMOS switch is used in the positive side, and an NMOS switch is used in the negative side, so that the supply voltage requirement of the comparator is reduced. Meanwhile, to avoid reverse current through the body diode, the MOSFET must be connected in a way such that the body diode is oriented as shown in Figure 4. The parallel connection of the MOSFET body diode and the active diode also helps pre-charge the load before startup of the circuit. The W/L ratio of the PMOS and NMOS are 1,500/1 in μm.

The comparators are input-powered directly by the AC input (V_{IN}). The power supply of the first stage (VDD1 or VSS1) is connected to the input through an external diode (D_1 or D_2, respectively). The diodes are required because the parasitic diodes between substrate and n-well will be turned on when the substrate is not connected to the lowest voltage of the circuit. D_1 and D_2 are connected in the direction to prevent any reverse current flowing from the substrate to the circuit. Since the diodes are not in the signal path, no additional conduction losses are induced.

Half-wave AC/DC converter

Although the output from the voltage doubler is DC at open-load due to the capacitors (C_1 and C_2), there will be an increasing ripple on this DC voltage when the circuit is loaded and the load current (I_{LOAD}) increases. The ripple frequency is much lower than the switching frequency of the DC/DC controller, and therefore it will not cause any

stability problem. However, the voltage sag, caused by the load-dependent ripple, makes the input-powered design challenging, because the DC/DC controller requires sufficient rail-to-rail voltage to function.

To overcome the voltage sag and ripple that arise on V_P with heavy load currents, a half-wave AC/DC converter is used as an auxiliary rectifier, which generates a low-ripple supply voltage (V_A) for the DC/DC controller. The more stable voltage V_A improves the overall circuit's minimum AC input voltage by providing a load-independent supply to the DC/DC converter (currently the minimum AC input is 1.2 V_{pk} at 3.7 V constant-voltage (CV) load).

The auxiliary rectifier employs the same design of positive-side voltage doubler, as shown in Figure 5. The active diode comprises a comparator and a PMOS switch. The output DC voltage (V_P) is stored in the output capacitor (C_3). Compared with a full-wave rectifier topology, the half-wave topology has been shown to deliver more power to the load in electrodynamic energy harvesting circuits where diode forward voltage drop is significant (Rao and Arnold 2011). The comparator is input-powered by connecting the power supply to the input through a diode D_3. The diode is needed to prevent turn-on of the parasitic diodes (silicon substrate to n-well) when the input AC voltage is lower than the circuit ground.

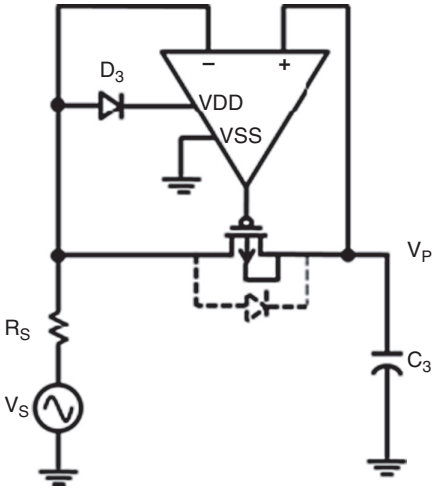


Figure 5 Schematic of the AC/DC converter

DC/DC stage

A switched-mode step-up DC/DC converter (also called boost converter) is designed to boost the rectified voltage to a usable level. The circuit diagram of the input-powered boost converter is shown in Figure 6, where an inductor L, a diode D, a switching transistor M_1, and an output capacitor C_{OUT} together form a basic boost converter. An on-chip DC/DC controller, highlighted by the dotted lines, is powered from the input (V_{IN}), much like the AC/DC converters in previous stage. This input-powered feature eliminates the need for external power supplies, reduces the pin count, and avoids standby power consumption, all of which are critical in energy harvesting applications.

The DC/DC controller uses pulse skip modulation (PSM) to achieve a regulated output DC voltage (V_{OUT}), in the presence of variation in the input voltage and load current. PSM uses both fixed duty cycle and fixed switching frequency, and therefore it regulates the output voltage through connecting or disconnecting the switching pulses with the switching transistor. Whenever the feedback signal is below the reference, the control switching pulse is applied so that the inductor starts charging and discharging energy, generating a higher output voltage until it reaches the reference. Although the regulation

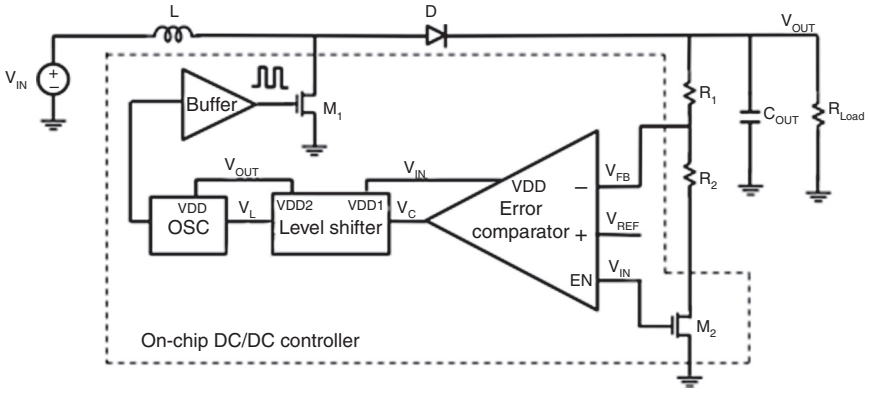


Figure 6 Block diagram of the input-powered boost converter

resolution of PSM is limited compared with conventional PWM (pulse-width modulation) and PFM (pulse-frequency modulation), it is chosen in this work for its decent efficiency at light loads and low circuit complexity.

A resistor ladder (R1 and R2) senses the output voltage level (V_{IN}) and generates a feedback voltage V_{FB} to be compared with the reference voltage V_{REF}. When V_{FB} is lower than V_{REF}, the error comparator output (V_C) goes high to activate an on-chip ring oscillator via a level shifter. The oscillator generates a switching pulse with fixed duty cycle and frequency, which drives the switching transistor M_1 through an on-chip buffer. Transistor M_1 cycles on and off to transfer power from the input to the output until V_{FB} is higher than V_{REF}, at which point V_C goes low and thus both the level shifter and the oscillator are disabled. M_1 remains off until sometime thereafter the load (R_{LOAD}) discharges the capacitor C_{OUT} and again V_{FB} drops below V_{REF}, the process restarts. In PSM, the inactive period increases at light load (i.e. small load current), which helps maintain low overall power consumption and a relatively high efficiency of the converter.

Note that a NMOS transistor M_2 is added into the resistor divider ladder, used to cut off the leakage path during standby mode. When V_A is below the NMOS threshold voltage, which is around 0.7 V in the 0.5 μm CMOS process, M_2 turns off and prevents any leakage current flowing through the resistor divider.

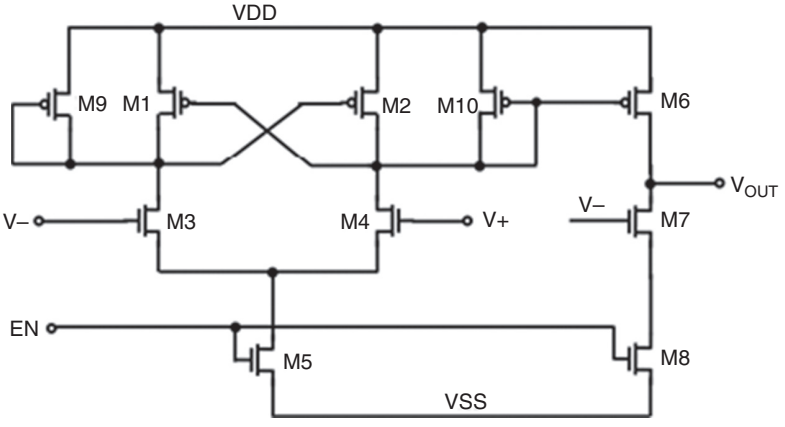
To avoid discharging the load when the circuit is in standby mode, the comparator in the controller circuit is input-powered by the converter's input (V_{IN}). Although the oscillator, the level shifter, and the buffer are powered or partially powered by the output voltage (V_{OUT}), these circuits will not consume static power when they are not active. The clock generator (OSC) and the buffer are the same with the previous publication (Rao and Arnold 2011) and will not be repeated here. The transistor-level design of the level shifter and the error comparator will be presented in the following.

Error comparator

As shown in Figure 7, a two-stage latching error comparator is designed, with the transistor size listed in μm. The NMOS differential pair (M3 and M4) in the first stage is chosen for its lower input common-mode range, with a large size to reduce the offset. The cross-coupled PMOS (M1 and M2) uses the minimum-size transistors to make the latch status swap easily when the input changes. The PMOS transistor pair is further weakened by adding another two diode-connected PMOS transistors (M9 and M10). The bias current is controlled by the input signal EN through NMOS transistors (M5 and M8). The pull-up PMOS (M6) in the second stage is sized large enough to make sure the output (V_{OUT}) is close to VDD when it is turned on. NMOS transistor M7 has the same size with input transistors (M3 and M4), to reduce the systematic offset from the second stage. Both EN and VDD are connected to the DC input (V_{IN}) of the boost converter, allowing the circuit to enter standby mode with no static current when EN is too low to turn on the bias transistors, or when VDD is not providing enough headroom for the comparator to work.

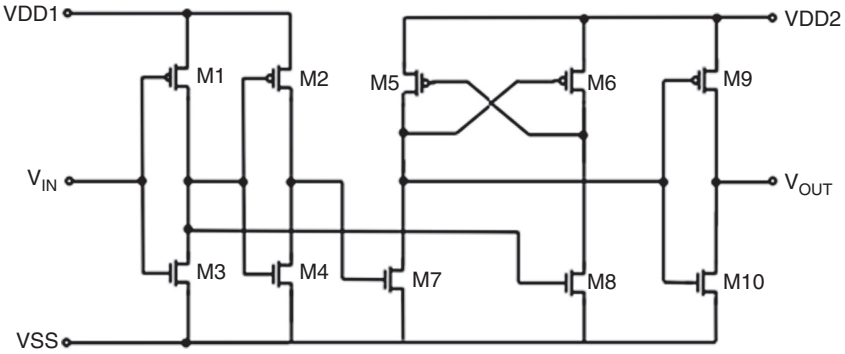
Level shifter

One of the main conduction losses in the DC/DC converter is the conduction loss of the switching transistor (i.e. M_1 in Figure 6). It becomes even worse in the input-powered design, where the switching pulse swing is uplimited by the input V_{IN}, and thus M_1 may not be fully turned on when V_{IN} is low. To solve this problem, a level



Transistor	W/L
M1–2, M8–10	1.5/0.6
M3–4, M7	15/0.6
M6	9/0.6
M5	3/0.6

Figure 7 Schematic of the error comparator



Transistor	W/L
M1, M2, M9	6/0.6
M3, M4, M10	3/0.6
M5, M6	1.5/12
M7, M8	30/0.6

Figure 8 Schematic of the level shifter

shifter is introduced to reduce the conduction loss of the switching transistor by increasing the voltage swing of the switching pulse on its gate.

Figure 8 gives the schematic of the level shifter with the transistor size in μm. The level shifter circuit shifts the logic "1" voltage from VDD1 to VDD2 by cross-connected PMOS latch (M5 and M6), whereas the logic "0" voltage remains unchanged at VSS. As a result, the input (V_{IN}) and the output (V_{OUT}) digital signals have the same frequency and phase, except that the voltage swings change from the input VDD (VDD1) to the output VDD (VDD2). The two inverters (M1 and M3, M2 and M4) are powered by the VDD1, generating sharp digital pulses to control the gates of M8 and M7, separately.

The latch stage and the output inverter (M9 and M10) are powered by VDD2, which will be connected to the boost converter output (V_{OUT}), as shown in Figure 8. Although these circuits are not strictly input-powered, they do not consume any static power when there is no input switching pulse. Therefore, the level shifter can enter sleep mode with no static power when the input (VDD1) is too low to supply enough rail-to-rail voltage, or there is no input pulse from the error comparator.

Considering logic 1 voltage of the input signal (V_{IN}) is relatively low (i.e. VDD1 is close to 1 V), strong NMOS transistors (M7 and M8) and weak PMOS transistors (M5 and M6) are sized to make sure the drain of M7 can be pulled down to VSS when VIN is high. Simulation result shows that the level shifter can work with VDD1 ranging from 1 V to 3 V, and VDD2 ranging from 3 V to 4.5 V.

Circuit fabrication

All of the above circuits are fabricated in silicon using an On-Semi 3M-2P 0.5-μm CMOS process. Figure 9(a) shows the voltage doubler chipset, with a size of 1.6 mm by 1.6 mm, packaged into one SOIC16 package. Figure 9(b) shows the DC/DC controller die, with a size of 1.6 mm by 1.6 mm, packaged in a SOIC 24 package. Both chips are covered by glass lids. Note that due to limitations of the MOSIS On-Semi 0.5-μm CMOS process (MOSIS AMI 0.5 μm Process 2013), several different dies are used to implement the AC/DC and DC/DC integrated circuits. However, using advanced twin-well process in the future, the entire interface circuit, including the voltage doubler chipset and the DC/DC controller chip, can be implemented on the same substrate in a single die. Therefore a smaller circuit size can be expected.

Table 1 lists all the other discrete components used in the interface circuit other than the circuit chip. It is important to acknowledge that a commercial button cell

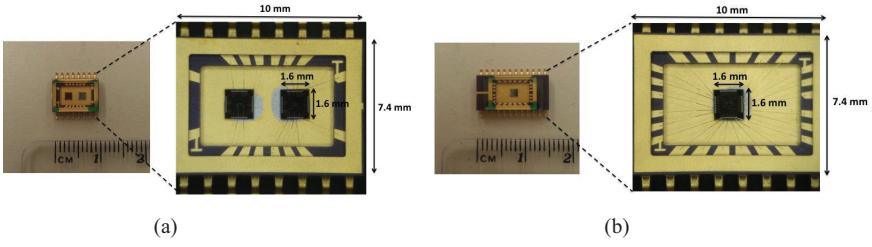


Figure 9 Micrograph of the interface circuit chips: (a) voltage doubler and (b) DC/DC controller

Table 1 List of discrete components in the system

Type	Name	Implementation
Inductor	L	22 μH
Diode	D	NSR0320 (On Semiconductor NSR0320 20V 1A low VF Schottky diode 2014)
Capacitor	C1, C2, C3, COUT	220 μF
Resistor	R1, R2	R1: 3 M; R2: 1 MΩ

battery with nominal voltage of 1.5 V is used to provide the reference voltage (V_{REF}) for the DC/DC controller, because there is no on-chip reference circuit. Note that this battery is connected to the gate of a MOSFET, and therefore the power consumption from this battery is negligible. In future designs, this battery can be replaced by an on-chip bandgap reference circuit.

Energy storage

In this design where the system size is strictly limited, a rechargeable lithium-ion (Li-ion) battery is used as the energy storage element. A Li-ion battery is chosen here not only because of its small size, light weight, and good energy density, but also because it has no memory effect and slow self-discharge rate. However, Li-ion batteries should be handled with caution, especially in high temperatures, because they can easily ignite or explode. A commercial Li-ion polymer rechargeable battery with nominal voltage of 3.7 V and maximum capacity of 65 mA h is used (Tenergy Li-ion polymer 3.7V 65mAh rechargeable battery 2013). The battery has a smaller size (23 mm × 12 mm × 4 mm) and a longer life time (up to 500 cycles charge/discharge) than conventional rechargeable cells. It has a built-in self-protection circuit to avoid over-charge or over-discharge.

System prototype

The interface chips, capacitors, diodes, and inductor are soldered on the top PCB1 as indicated in Figure 10, whereas the button battery and the rechargeable battery are mounted on the bottom PCB2. These two round PCBs with 3.2 cm diameters are mounted on top and bottom surfaces of the harvester to form the complete harvesting system. The system components are wrapped with electrical tape, as shown in Figure 11. The prototype system has a cylinder structure with 6.3-cm height and 3.8-cm

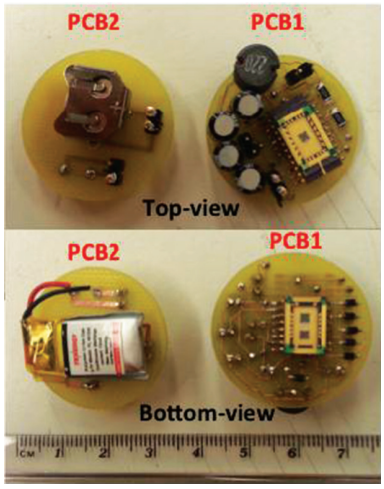


Figure 10 Photographs of the circuit boards

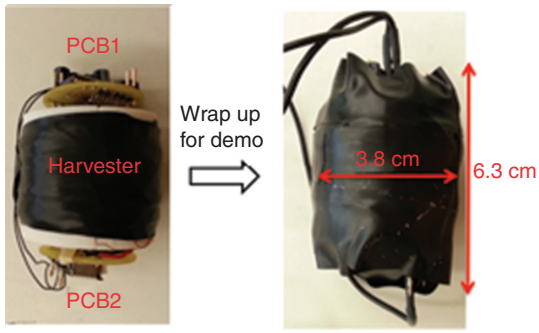


Figure 11 Photographs of the system

diameter, leading to a total volume of about 70 cm^3 and a total weight of 81 g.

Experimental results

In the experiment, the interface circuit is first bench-top characterized by an ideal sine wave to mimic the output voltage from a real energy harvester. The full system prototype is then mounted on a human body and characterized under normal human movements, such as jogging, walking, and cycling.

Interface circuit characterization

The measurement setup of the interface circuit is shown in Figure 12. The AC input is from a function generator (Agilent 33120A), and the reference voltage (V_{REF}) to the DC/DC controller is provided by a DC power supply

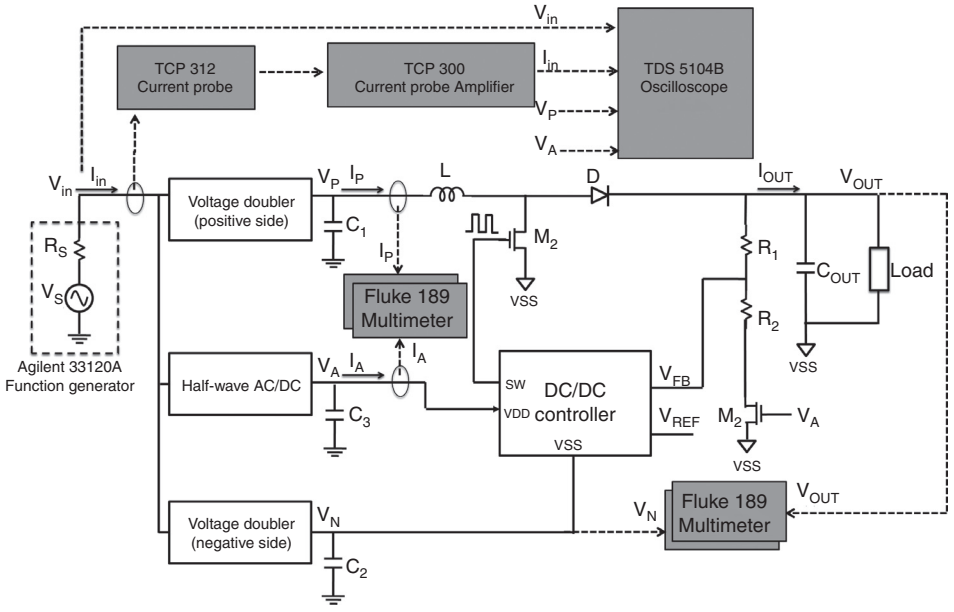


Figure 12 Measurement setup of the complete input-powered interface circuit

(Agilent E3616A). The input voltage $v_{in}(t)$ is measured by an oscilloscope (Tektronix TDS5104B). The input current $i_{in}(t)$ is first sensed by a current probe (Tektronix TCP312) and then amplified by a current amplifier (Tektronix TCP300). Both the input voltage and the input current waveforms are displayed on the same oscilloscope, so that the time-averaging input power can be calculated by the mathematic function of the oscilloscope.

The output from the positive-side AC/DC converter (V_P) and the half-wave AC/DC converter (V_A) are measured by the other two channels of the oscilloscope. The output DC current from the voltage doubler (I_P) and the half-wave AC/DC converter (I_A) are measured by Fluke189 digital multimeters. Another two multimeters are used to measure the DC output voltages from the negative-side voltage doubler and the DC/DC converter. A BK Precision 8500 serves as a CV electronic load.

Output power

At open-load where there is no load current, the system turns on when the AC input is above 1 V_{pk} and turns off when the AC input drops below about 600 mV_{pk}. With a 3.7 V CV load, Figure 13 shows the measured output power as a function of increasing input amplitude $V_{in,pk}$. The minimum AC input voltage to wake up the circuit with a 3.7 V load is 1.2 V with a corresponding load power of 1.1 mW. For increasing input voltage, the power delivered to the load increases up to 22.6 mW for a 3.0 $V_{in,pk}$ input. Note that the breakdown voltage of 0.5 μm CMOS process limits the maximum measured input amplitude to 3.0 V.

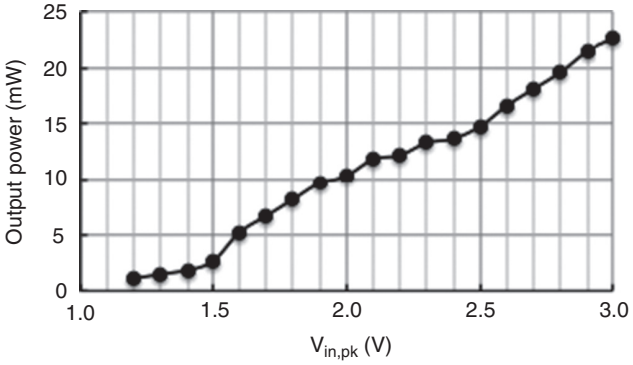


Figure 13 Power delivered to 3.7 V battery at different input voltage amplitudes

Power efficiency

According to the measurement setup shown in Figure 12, the power efficiency of the AC/DC stage ($\eta_{AC/DC}$), the DC/DC stage ($\eta_{DC/DC}$) and the overall interface circuit ($\eta_{interface}$) can be calculated as

$$\eta_{AC/DC} = \frac{P_{AC/DC}}{P_{in}} = \frac{(V_P - V_N) \times I_P + V_A \times I_A}{\frac{1}{T}\int_0^T [v_{in}(t) \times i_{in}(t)]dt} \quad [1]$$

$$\eta_{DC/DC} = \frac{P_{out}}{P_{AC/DC}} = \frac{V_{OUT} \times I_{OUT}}{(V_P - V_N) \times I_P + V_A \times I_A} \quad [2]$$

$$\eta_{interface} = \frac{P_{out}}{P_{in}} = \frac{V_{OUT} \times I_{OUT}}{\frac{1}{T}\int_0^T [v_{in}(t) \times i_{in}(t)]dt} \quad [3]$$

where $v_{in}(t)$ and $i_{in}(t)$ are instantaneous input voltage and current (AC), V_P–V_N and I_P are the output voltage and current (DC) of the voltage doubler, V_A and I_A are the output voltage and current (DC) of the half-wave AC/DC converter, and V_{OUT} and I_{OUT} are the output voltage and current (DC) of the system, respectively. The time T is the duration of measurement, chosen to be larger than at least 10 times the input period.

Figure 14 shows the bench-top measurement result of circuit power efficiencies of the AC/DC stage, the DC/DC converter, and the overall interface circuit at different input voltage amplitudes. The overall efficiency is above 60% for input voltages >2.5 V_{pk}. In this design, the overall efficiency is limited by both the AC/DC and the DC/DC stage. For instance, with a 20 Hz sine wave with input amplitude of 2.6 V and regulated DC output of 3.7 V, the system achieves an overall efficiency of 61% when delivering 16.7 mW of output power; the efficiency of the AC/DC stage and the DC/DC stage are 84% and 73%, respectively.

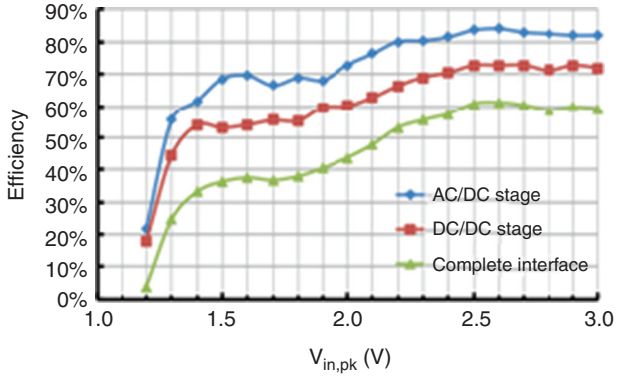


Figure 14 Circuit efficiency at different input voltage amplitudes and a 3.7 V regulated DC output

The AC/DC converter efficiency increases with the input amplitude because conduction loss decreases with smaller R_{ds}(on) of switching transistors (e.g. switch MOSFETs in the rectifiers). For the boost converter, the power efficiency at light load is poor because of the switching loss and the fixed loss of the controller circuit. However, at medium-heavy load, power loss is primarily conduction loss of the switching MOS (e.g. M_1), which is proportional to the square of output current. Therefore when the output current increases, the power efficiency increases because of the reduced impact of the switching loss and the fixed loss.

System measurement

The energy reclamation performance of the complete energy harvesting system is then measured when subjected to real human activities. In the experiments, the system is attached to a person's ankle, wrist, or upper arm. These locations are chosen for two reasons. The first reason is that more motion/vibrations are expected at these locations, and thus more energy can be harvested (Peters, Ortmanns, and Manoli 2007). Another reason is that to attach the system on these locations will not cause too much discomfort in daily human activities, which is important for future applications. Because different people may have different gaits in daily activities, the generated energy will vary from person to person. Therefore, in the experiment, the same person is tested for all the activities, so that the result is consistent among different locations and movements.

The system energy reclamation is measured for three types of movements: walking, jogging, and cycling. Walking and jogging are conducted on a treadmill, while cycling is performed on a stationary cycling machine. By doing so, the speed of each activity is accurately controlled and replicated. Each activity type is tested for 10-min duration and is repeated by attaching the system to the different parts of the body. To quantify the harvested energy, the battery voltage is measured at 1-min intervals during the activity. Comparing the voltages to the separately measured battery charging curve at 100 μA charging current, the total energy delivered from the system to the battery is estimated.

Delivered energy

Figure 15(a) shows the estimated energy delivered to the battery versus time when the system is mounted on the ankle for jogging, walking, and cycling. Comparing these three activities, the most accumulated energy of 142 mJ is delivered after 10 min of jogging. This result is within our expectation because jogging generates larger vibration accelerations than walking and cycling. Similarly, Figure 15(b) plots the energy delivered during jogging when the system is mounted at ankle, arm, and wrist of the human body, among which the most significant energy of 142 mJ is detected at the wrist. Note that in

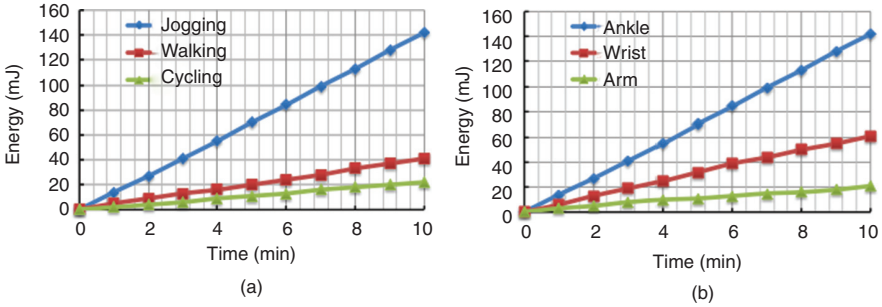


Figure 15 Energy delivered to the battery: (a) from human ankle and (b) from jogging

both figures, the energy delivered increases almost linearly with the time of human movements, because the speed of each human activity keeps constant.

Average output power

The average harvested power can be estimated by calculating the slope of the lines in Figure 15. Table 2 summarizes the measurement results. The average power delivered to the battery ranges from 30 μW to 234 μW for the different configurations tested. When mounted on the ankle, the maximum power of 234 μW occurs for jogging, resulting a power density of 3.34 μW/cm^3. Due to the relatively small upper-body vibrations (Elvin and Elvin 2012), no significant power is measured at the arm during walking and cycling, and the same for the wrist during cycling. This is attributed to the energy harvester not generating sufficient AC voltage amplitude for the interface circuitry to function.

Table 2 Measured average power delivered to the battery

	Ankle	Wrist	Arm
Jogging	234 μW	100 μW	30 μW
Walking	67 μW	33 μW	N/A
Cycling	34 μW	N/A	N/A

Conclusions

The primary contribution of this work is the development of a completely self-sufficient vibrational energy system for passively harvesting power from natural human movements. The design considerations and experimental results of the energy harvester, interface circuit, and energy storage were explored and characterized in detail. The energy harvesting system was demonstrated, and the power delivered to a rechargeable battery was characterized in real applications.

The measurements show that a maximum average power of 234 μW is delivered to the battery during jogging when the system is mounted on the ankle. For a system volume of 70 cm^3, the system achieves a net power density of 3.3 μW/cm^3. Compared with a previous design (Rao, Cheng, and Arnold 2013), the system here achieves 10% higher net power density in 30% smaller volume.

The system can be further improved by shrinking the size and increasing the output power. For example, by migrating the circuit to a more advanced CMOS technology, the minimum AC voltage requirement for the interface circuit is less restricted, allowing a smaller harvester size in the system. The spherical energy harvester design can also be improved by optimizing the structure and the coil winding. Furthermore, impedance matching techniques can be implemented to maximize the output power of the system, especially when the transducer type and the load conditions are pre-defined.

Acknowledgment: This work was supported in part by Texas Instruments via a fellowship for Yuan Rao.

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