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Fabrication and characterization of CMOS-compatible perforated micromembranes for biomedical applications

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Abstract: We report the optimized wafer-scale fabrication of microporous membranes for applications in the biomedical field such as cell filtration. Existing similar devices can mostly not be integrated on CMOS circuits or mass fabricated. Both is enabled here by the exclusive use of scalable and low temperature microsystems technology methods on silicon wafers. The successfully manufactured devices are characterized with regard to the feasibility of an integrated clogging detection or captured cell counter. The results from electrochemical measurements across the chips match the calculations from a corresponding theoretical model well, verifying the described concept. Further electrical functionalities may thus be integrated into the micromembrane device in the future, equipping it for new applications and allowing a more efficient solution for existing tasks of similar devices.

Keywords: Micromembrane, microperforation, microfluidics, filtration.

1 Introduction

Microperforated membranes are used in diverse biomedical applications. For instance, circulating tumor cells can be detected, enumerated, captured, isolated and characterized using such devices [1–4]. Besides filtering cells from blood, perforated micromembranes are also used to model vascular walls or the blood-brain barrier [5–7]. The transport of cells across these barriers or other interactions with the blood and its contents can thus be studied. Similarly, microporous membranes are used in organs-on-chips to separate two cell cultures while facilitating mass transfer and communication between

the two sides [8]. Thus, different processes in organs are modeled and investigated, e.g. with regard to their response to new drugs. Other applications of perforated micromembranes include drug delivery [9], cell fractionation [10] and the detection of pathogens [11]. Furthermore, combining filtration with electrical functionalities in one device enables further applications and increased efficiency compared to serial processing. Zheng et al. [4], for instance, integrated electrodes into the membrane pores to enable in situ electrolysis and subsequent analysis of the genome of captured cells. Besides stimulation or poration, sensing the amount of captured cells or the progress of the device clogging may also be helpful.

Due to the wide field of applications, many fabrication processes for microperforated membranes have been proposed and demonstrated – including wafer-scale microsystems technology methods. Integrating the described membranes on complementary metal oxide semiconductor (CMOS) wafers, however, remains a challenge. We recently reported the successful implementation of a CMOS-compatible fabrication method for perforated membranes which enables future integration of electrical functionalities into the devices [12]. Here, we optimize the fabrication, characterize the devices electrochemically and prove the concept for a first such functionality.

2 Methods

2.1 Device fabrication

Perforated membranes with backside cavities are fabricated using the process depicted in Fig. 1. The procedure described before [12] is extended and optimized. An etch stopping layer and a membrane are first deposited on a silicon wafer with a diameter of 200 mm and a thickness of 750 μm . The membrane is structured by reactive ion etching and a protection layer is deposited on top. Before the backside cavities are etched, however, the wafers are ground down to a thickness of 450 μm . Thinning the wafers reduces the aspect ratio and thus the complexity of the following deep reactive ion etching (DRIE) process. A hard mask is deposited and structured and the cavities are subsequently created in a Bosch process. The etch is

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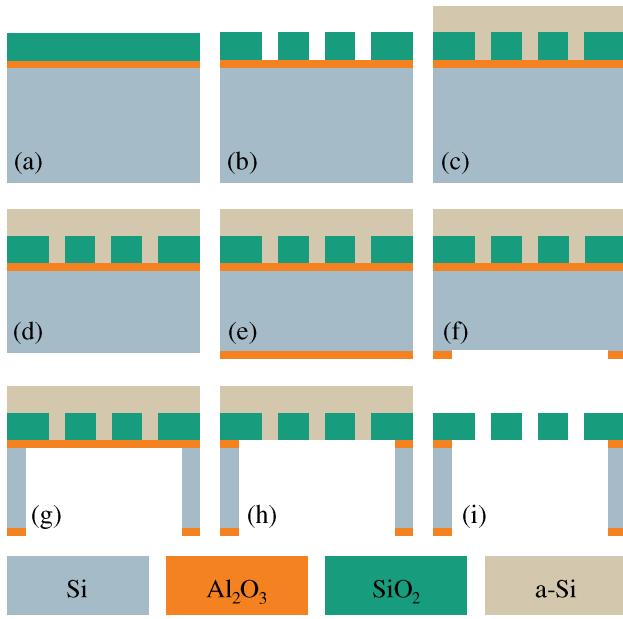


Fig. 1: Fabrication concept of chips with perforated micromembranes connected to backside cavities. Atomic layer deposition (ALD) of an etch stopping layer, chemical vapor deposition (CVD) of the membrane material (a), structuring of the membranes (b), CVD of a protection layer (c), grinding of the wafer substrate (d), ALD of a hard mask (e), structuring of the hard mask (f), DRIE of backside cavities (g), removal of the etch stopping layer (h) and removal of the protection layer (i).

stopped on the stopping layer which is subsequently removed using ion beam etching. Finally, the protection layer on top of the membrane is removed in a chemical vapor etching step.

For comparison and analysis, several different variations of the described device are fabricated. The number of pores per membrane is varied as well as the pore diameter and the spacing between pores. Moreover, devices with a thickness of 750 μm , i.e. skipping the grinding step (d), are fabricated to analyze the effects of thinning.

2.2 Electrochemical measurements

The resulting chips are mounted in a test setup consisting of two containers filled with electrolyte solution (KCl in deionized water). Each container has an opening almost matching the size of the chips so that the cavities and pores are the only connection between the two reservoirs. Inserting an Ag/AgCl electrode in each of the containers and applying a voltage thus allows the measurement of ion currents flowing through the cavities and pores. The results from linear voltage sweeps can subsequently be compared to calculations from a theoretical model.

2.3 Chip resistance estimation

Simplified, both the cavities and the pores are considered isolated conductors in which the electrolyte solution acts as the conductive material. The resistance of such a conductor $R_{\text{Conductor}}$ can be calculated according to equation 1 where l is the length and r is the inner radius of the hollow structure. The conductivity of the electrolyte solution κ is calculated from test and calibration measurements before each experiment.

$$R_{\text{Conductor}} = \frac{l}{\kappa \pi r^2}. \quad (1)$$

Additionally, the access resistance R_A is calculated using equation 2. This accounts for the resistance caused by the limited conductivity of the external electrolyte solution and considers the inner orifice radius limiting the flow of ions from the outer bath solution to the inner filling solution [13, 14].

$$R_A = \frac{1}{4\kappa r}. \quad (2)$$

On a given chip, several cavities (index c) are connected in parallel. An individual cavity, in turn, is serially connected to several parallel pores (index p). Therefore, the resistance of the entire chip may be estimated by equation 3.

$$R_{\text{Chip}} = \frac{1}{n_c \kappa} \left(\frac{l_p}{n_p \pi r_p^2} + \frac{1}{4n_p r_p} + \frac{l_c}{\pi r_c^2} + \frac{1}{4r_c} \right). \quad (3)$$

3 Results

3.1 Microscopy analysis

The different design variations described in subsection 2.1 were successfully fabricated. The freestanding membranes are stable and the etch stopping layer could be removed without compromising the integrity of the membranes. Thus, the cavities eventually span the entire wafer and connect the pores to the backside of the chips. The scanning electron microscopy images in Fig. 2 show a chip with the original wafer thickness (a) and a thinned one (b). In comparison, the cavity walls of the thinned chip are smoother and the enlargements at the cavity entrance are smaller and more regular. The enlargement underneath the membrane, however, has a similar shape in both cases.

Moreover, microscopy images of three different geometry variations are shown in Fig. 2, demonstrating the integrity of the membranes. Both the cavities and the pores are visible in the top view of the membranes with the cavities showing as green circular shapes around the pores.

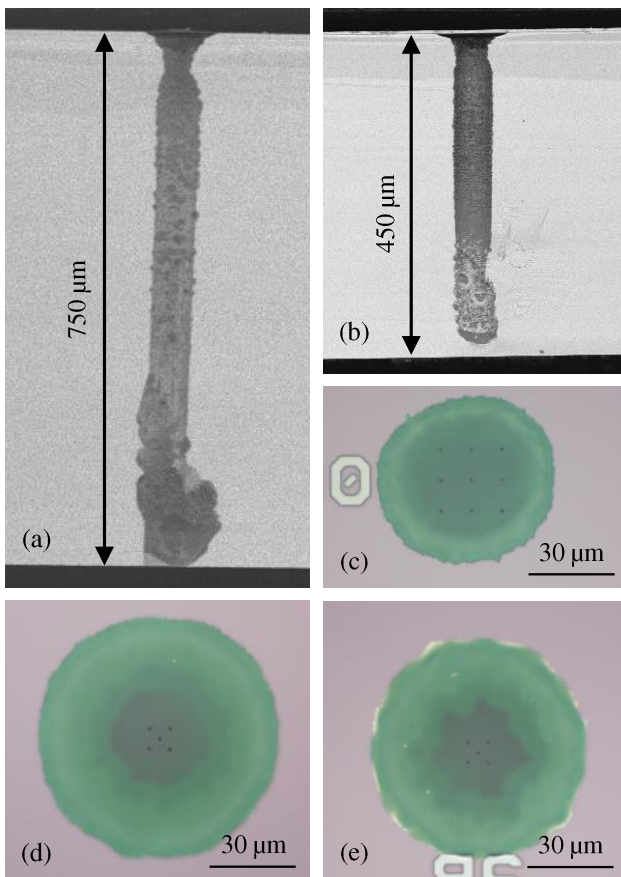


Fig. 2: Images of the resulting chips. Cross-sectional scanning electron micrographs of cavities in a chip with 750 μm thickness (a) and in a thinned chip (b). Top-views of membranes containing 9 pores with 200 nm radius (c), 5 pores with 200 nm radius (d) and 5 pores with 450 nm radius. The backside cavities are visible through the membranes as green circles.

Tab. 1: Characteristics of the measured chips. For all the chips measured here, the number of cavities n_c is 16, the inner radius of an individual cavity r_c is 25 μm , the length of an individual cavity l_c is 750 μm and the length of an individual pore l_p is 2.8 μm . The number of pores per cavity n_p and the radius of the individual pores r_p vary between the listed chips resulting in different chip resistances R_{Chip} .

n_p	r_p (nm)	$R_{\text{Chip,calculated}}$ (k Ω)	$R_{\text{Chip,measured}}$ (k Ω)
5	200	271	271.4 ± 1.3
5	450	74	75.1 ± 2.6
9	200	128	132 ± 27

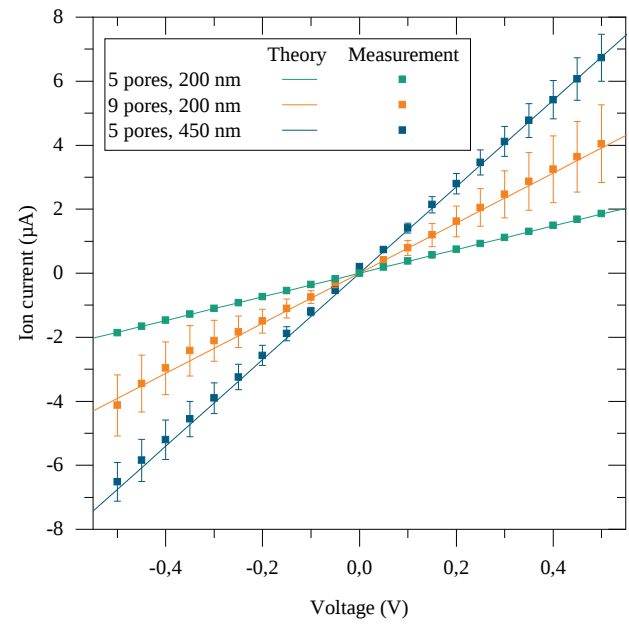


Fig. 3: Ion current measurements from voltage sweeps and the corresponding graphs from the analytical model for three different chip designs. Five separate sweeps were performed for each design.

3.2 Comparison of electrochemical measurements and theory

For the three chip designs depicted in Fig. 2 (c) to (e), the results from electrochemical measurements and calculations using equation 3 are shown in Tab. 1 and Fig. 3. The measured I-V-curves are approximately linear in all three cases and the mean resistances calculated from the measurements vary by less than 4 % from the analytically calculated resistances. Nevertheless, the standard deviation varies significantly between the three chip designs. The chip with 9 pores per cavity shows the highest standard deviation between individual measurements and the greatest difference between measured and calculated resistance. By contrast, the chip with $n_p = 5$ and $r_p = 200$ nm shows the lowest variations. However, the data quantity is not sufficient for a reliable statistical evaluation.

4 Discussion and Conclusion

In principle, the fabrication of the perforated micromembranes with backside cavities works reliably. As described before [12], the proposed procedure is compatible with CMOS technology and flexible regarding several geometric parameters such as number of pores, membrane thickness, pore diameter, etc. Therefore, the production is scalable and the devices can

be precisely adjusted to the requirements of different applications. In an additional processing step, the resulting chip can be coated by a thin ALD layer to also adapt the surface properties and ensure biocompatibility. Furthermore, thinning the substrate is useful not only for improving the fabrication process. The aspect ratio of the backside cavity is reduced which reduces both the required etch time and the sidewall enlargements. However, the shorter cavity also reduces the resistance of the chip (see equations 1 and 3), the pressure required to pump a fluid through the chip as well as the diffusion distance for particles crossing the device.

Moreover, the electrochemical measurements match the theoretical approximations well. The chip with 9 pores can be distinguished from the chip with 5 pores based on the measurements shown in Fig. 3. Likewise, the different diameters of the pores lead to distinct I-V-curves as well. It may thus be inferred from measurements, how many pores of which diameter the membranes contain. In filtration applications, this may allow the detection of clogging via electrical measurements or an estimation of the number of captured cells. However, the standard deviations as shown in Fig. 3 and Tab. 1 are too high to allow detection with precise single pore resolution. Therefore, a refinement of both the measurement setup and the theoretical model is necessary. For instance, the electrochemical behavior of the electrodes and the electrolyte solution varied between measurements so that a calibration was necessary before each voltage sweep. Ensuring steady external conditions (e.g. constant temperature, commercial electrodes, etc.) may improve measurements and reduce the need for frequent calibrations. With a revised measurement setup, more data need to be collected to statistically validate the findings discussed here. Furthermore, the theoretical model does not account for capacitive effects or parasitic currents at the membrane. These effects were neglected as they were assumed to be small compared to the conduction of ions through the electrolyte solution. However, it needs to be evaluated whether the predictions can be improved by including these nonlinearities in the analytical model.

In total, the feasibility of both the CMOS-compatible fabrication of perforated micromembranes and the pore characterization based on electrochemical measurements were successfully shown. This demonstrates only one of many possible electrical functionalities which can be integrated into the described devices in the future to broaden their potential applications.

Author Statement

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