Lena Bleck*, Andreas Heid and Rene von Metzen

Silicone-based Chip-in-Foil System

Abstract: Aiming at devices for bioelectronic medicine, this paper proposes a die embedding process for the fabrication of flexible smart implants. By combining thinned bare dies with a polymeric encapsulation, completely flexible implants can be designed. The dies are encapsulated using a flip-chip process and a backfilling with silicone rubber. A completely even surface without detectable edge between the chip and the surrounding polymer substrate is achieved by gluing the chips face-down onto a polyimide-covered substrate. The backside is coated with silicone rubber and a second carrier substrate is attached. Removing the first substrate subsequent to curing of the silicone leads to chips located under a continuous polyimide layer, enabling the use of micro-technology for further processing steps. A custom-made test chip is proposed that enables the evaluation of the mechanical and chemical stability of the system.

Keywords: chip-in-foil, smart implant, neural implant, electroceuticals, bioelectronics medicine, active implant, miniaturized, die embedding

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1 Introduction

Nowadays, a lot of research focusses on the use of electroceuticals as a substitution of systemic drugs. The aims are the minimization of side effects in the therapy of multiple disorders and diseases as well as opening the way to new treatments [1]. By employing an electric treatment, it is hoped to gain a localized effect, without effecting the surrounding environment. However, based on the delicate nature and often limited spatial resolution of neuronal tissue this necessitates the development of flexible miniaturized electronics for the electrostimulation and sensing [2]. To circumvent a mechanical mismatch between the body tissue and the implanted devices while maintaining a high number of electrode leads, the use of a non-hermetically encapsulated foil implant has proven beneficial [3]. Other than the higher flexibility compared to a hermetic housing, this also obviates the need for feedthroughs. More complex electronics can be achieved by placing complementary metal oxide semiconductor (CMOS) chips in the foil implant. By grinding them to a residual thickness of around 30 µm, the chip itself turns bendable [4]. However, for the microfabrication of conducting tracks, even a step of some µm can prove critical, leading to cracks in the metal [5]. Therefore, one of the foci has to be set at achieving a flat surface despite the residual height of the CMOS chip. Based on the limited number of flexible polymers for medical applications, silicone rubber is selected based on its higher processing thickness combined with the good biostability. However, due to the incompatibility with most thin-film processes, a flip-chip process is envisioned that combines micro structuring with thicker silicone rubber films.

2 Test chip

For the chip embedding process, special microchips are devised hosting analog test structures to determine both the quality of the electric contact as well as the biostability in an in-vitro test setup. The passive test chips (PTC) are 4.7 mm

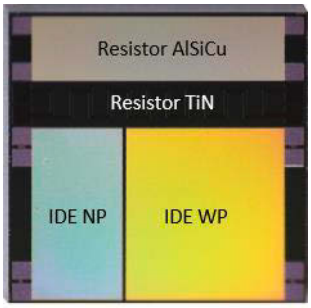

Figure 1: Figure 1: Layout of the passive test chip containing four different test structures fabricated using standard CMOS technologies. A resistor structure designed by meandering the tracks is fabricated using AlSiCu and TiN. The IDEs are designed with passivation (WP) and without passivation (NP).

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Table 1: Average impedance with standard deviation of the structures on the PTC for three chips, measured using impedance spectroscopy and a needle prober.

Structure	Impedance at 1 kHz
Resistor AlSiCu	9531.13 Ω ± 7.96 Ω
Resistor TiN	18.7 Ω ± 1.08 Ω
IDE NP	3.51 MΩ ± 40.8 kΩ
IDE WP	890.1 kΩ ± 3.05 kΩ

by 4.7 mm with a thickness of around 30 µm after grinding (Fig. 1). They are fabricated at the Institut für Mikroelektronik Stuttgart (IMS) using a standard 0.5 µm CMOS-technology. Two of the four test structures are meandered resistors, of which one is fabricated using the standard AlSiCu metallization and the other one is fabricated using the TiN pad material that is employed as via etch stop. They can be used to measure the corrosion of the conducting tracks and pads as well as the contact resistance to the chips. The other test structures are interdigital electrodes (IDE) with a finger width of 6 µm and distance of 1.2 µm. One of the IDEs is covered by the standard CMOS passivation of 300 nm SiO_2 and 550 nm Si_3N_4 (IDE WP), the passivation on top of the other IDE is removed using the etch process for the contact pads (IDE NP). This way, any failure of the encapsulation can be directly determined with and without the influence of the passivation. The parameters for the test structures are shown in Tab. 1. All structures offer the option of a 4-wire measurement.

3 Chip embedding

3.1 Flip-chip process

For the embedding of the PTCs into a foil system, a 4.9 by 4.9 mm² glass substrate is chosen as carrier substrate, which can be detached after all processing steps are completed. A 6-µm-thick Polyimide (PI) (PI-2611, DuPont, Wilmington, DE, USA) layer is spin-coated and cured at 350 °C (Fig. 2 A). Alignment marks used as fiducials for the chip placement are fabricated by depositing and structuring a 100-nm-thick titanium layer. The PTCs are glued face-down onto the PI using Epo-Tek 354 (Epoxy Technology Inc., Billerica, MA, USA) with a glue thickness of 5 µm to 10 µm. Additionally, spacer chips with a thickness of 200 µm and an overall size of 1.5 mm by 1.5 mm are glued into each of the corners of the glass substrate (Fig. 2 B). For the flip-chip process, a second glass substrate is coated with a metallization of 10 nm titanium, 200 nm platinum and 1000 nm of aluminum, covering all sides of the glass. The backside is then covered using Kapton tape (DuPont, Wilmington, DE, USA). Both substrates are then treated with atmospheric plasma for 90 s. Subsequently, a thin layer of the primer Dow Corning 1200 OS (Dow Corning, Midland, MI, USA) is applied by spin-coating at 1000 rpm for 15 s followed by a 2 h curing step at room temperature and a minimum humidity of 20 %. The silicone rubber Sylgard 184 (Dow Corning, Midland, MI, USA) is mixed in a ratio of 10:1 (base to curing agent) using a speed mixer at 2000 rpm. The substrate carrying the chips is placed in a petri dish and covered with the uncured silicone rubber, which is then degassed for 20 min using a vacuum chamber (Fig. 2 C). Subsequently the metal-coated substrate is placed on top, aligning both substrates carefully (Fig. 2 D). By placing a metal plate underneath the petri dish and a magnet on top of the metal substrate, both glass substrates are pressed together. The residual gap and therefore silicone layer thickness is determined by the spacer chips. The silicone rubber is cured at room temperature for two days to minimize shrinkage. After curing, the samples are detached from the petri dish by cutting around the edges of the substrate using a scalpel and peeling the Kapton from the substrate backside. The samples are then placed in de-ionized water (DIW) at 60 °C for 4 h. This detaches the PI from the carrier substrate, which can be easily removed with a tweezer. At this point, the chips are face-up under 5-µm-thick glue and a flat layer of 6-µm-thick PI (Fig. 2 E & F).

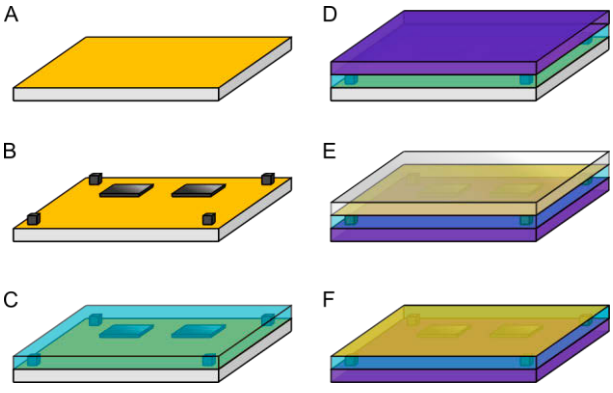

Figure 2: Schematic view of the chip embedding process. A PI-covered glass (A) is used as a substrate. The chips are glued face-down onto the PI (B) and covered with silicone rubber (C). A second glass is pressed onto the uncured silicone (D). After curing, the sample can be flipped (E) and the interface between glass and PI can be detached by placing in DIW (F).

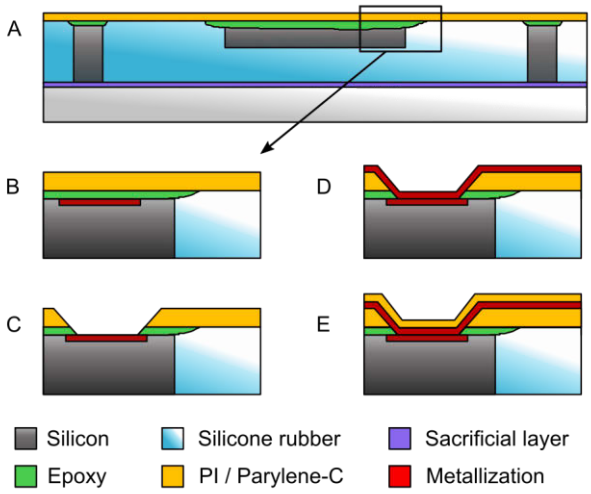

Figure 3: Schematic cross section of the embedded die (A) with a close-up (B) showing the etching of slanted vias (C) followed by a metallization step (D) and the final Parylene C encapsulation layer (E).

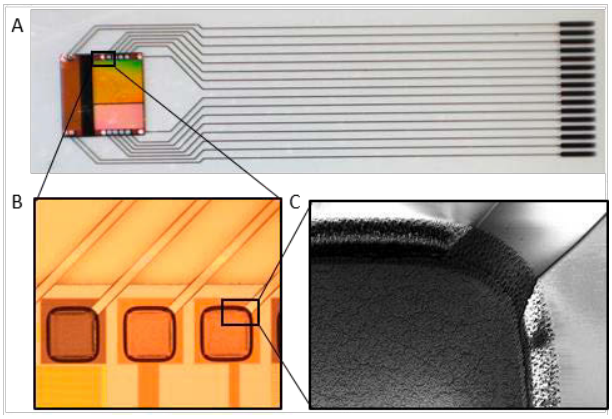

Figure 4: Picture of the embedded chip after contacting using TiPtTi metal tracks (A). Micrograph of the metal tracks covering the chip edge, showing no step in the metallization. A SEM picture of a via after the metallization (C) shows that the slanted via edge is completely metallized.

3.2 Micro structuration

To structure the surface of the substrate, a 40-µm-thick etch mask is fabricated using AZ IPS 6050 photo resist (Microchemicals GmbH, Ulm, Germany). The vias are etched using reactive ion etching (RIE) with oxygen plasma in a two-step process: The first step at 100 mTorr is employed to achieve a via with slanting edges while a second step at 50 mTorr cleans the etch residues from the contact pad. The resist is stripped by dipping in 80 °C hot DMSO (Microchemicals GmbH, Ulm, Germany) for 2 h followed by 5 min of ultrasonic (US) bath. The substrates are then metallized by sputter-depositing 10 nm titanium, 300 nm gold and 10 nm titanium. The metal is structures using RIE with a mixture of argon and CF4-plasma for the titanium and Ar-plasma for the gold. Prior to the deposition of a 3-µm-thick Parylene-C (Specialty Coating Systems, Indianapolis, IN, USA) layer, the samples are cleaned using argon and oxygen plasma and coated with the adhesion promoter A174 (Merck KGaA, Darmstadt, Germany). The contact pads for the connector are opened using RIE with oxygen plasma at 200 mTorr.

After the surface is structured, the overall contours of the samples are cut using a laser. The samples are then detached by electrochemically dissolving the aluminum layer surrounding the carrier substrate. This is achieved by placing the samples in 25 % saline solution and connecting them to a platinum counter electrode with a 0.5 V voltage applied. After several hours, the aluminum is completely in solution, leaving a non-attached chip-in-foil system.

4 Discussion

In this paper, a process for the embedding of ultra-thin silicon dies into a polymer foil is described, leading to a chip-in-foil system that is potentially suitable for medical implants (Fig. 4 A). One of the main issues targeted in this embedding process is the goal of having a surface with no detectable topography variations. As Govaerts et al have reported, having a gap between the chip surface and polymer substrate can lead to significant issues in the metallization. This is reported to be due to an uneven resist layer which causes gaps in the metallization [5]. As shown in Fig. 4 B, this can be successfully prevented by bridging any height differences with silicone rubber, leading to completely even metal tracks.

Compared to PI and Parylene-C, silicone rubber has proven suitable for the levelling of steps due to the non-conformal coating without any shrinkage. Additionally, the room temperature process is suitable for epoxy glues with a low temperature stability, needing considerably less safety precautions and processing effort compared to the benzocyclobentene compatible with PI curing temperatures [6].

One of the main drawbacks of silicone rubber is the incompatibly with most cleanroom processes. As is reported by Schüttler et al, one alternative is the structuring of silicone using a laser. However, this often damages the underlying metal structures [7], which severely limits the reliability of the combination of thin-film metallizations with overlaying silicone structures. By limiting the use of silicone to the backside of the chips, no structuring of the silicone rubber beyond the final contour lines is necessary, which enables the

use of standard RIE processes for via and metal etching (Fig. 4 C).

During the course of this technical development, the compatibility of all processes have been shown. However, both the mechanical stability of the device after detaching from the carrier substrate as well as the chemical stability to saline solution has not been investigated so far. Therefore breaking of the tracks at the chip-epoxy-silicone edge due to a mechanical mismatch cannot be ruled out until further testing has been concluded. Additionally, the long-term stability of the device has to be tested with respect to delamination, corrosion and swelling of the polymers. Nevertheless, a promising technology for the embedding of dies into biocompatible foil systems has been developed.

Author Statement

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References

[1] K. Famm, B. Litt, K. J. Tracey, E. S. Boyden, and M. Slaoui, "Drug discovery: a jump-start for electroceuticals," Nature, vol. 496, pp. 159-161, 2013.

[2] R. Biran, D. C. Martin, and P. A. Tresco, "Neuronal cell loss accompanies the brain tissue response to chronically implanted silicon microelectrode arrays," Experimental neurology, vol. 195, pp. 115-126, 2005.

[3] J.-U. Meyer, "Retina implant—a bioMEMS challenge," Sensors and Actuators A: Physical, vol. 97, pp. 1-9, 2002.

[4] J. N. Burghartz, W. Appel, C. Harendt, H. Rempp, H. Richter, and M. Zimmermann, "Ultra-thin chips and related applications, a new paradigm in silicon technology," in Solid State Device Research Conference, 2009. ESSDERC'09. Proceedings of the European, 2009, pp. 29-36.

[5] J. Govaerts, W. Christiaens, E. Bosman, and J. Vanfleteren, "Fabrication processes for embedding thin chips in flat flexible substrates," IEEE transactions on Advanced Packaging, vol. 32, pp. 77-83, 2009.

[6] W. Christiaens, E. Bosman, and J. Vanfleteren, "UTCP: A Novel Polyimide-Based Ultra-Thin Chip Packaging Technology," IEEE Transactions on Components and Packaging Technologies, vol. 33, pp. 754-760, 2010.

[7] M. Schuettler, S. Stiess, B. V. King, and G. J. Suaning, "Fabrication of implantable microelectrode arrays by laser cutting of silicone rubber and platinum foil," Journal of neural engineering, vol. 2, p. S121, 2005.