Biomed Tech 2013; 58 (Suppl. 1) © 2013 by Walter de Gruyter · Berlin · Boston. DOI 10.1515/bmt-2013-4367

A SUBSTRATE ISOLATED LDO FOR AN INDUCTIVELY POWERED RETINAL IMPLANT

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Abstract: *A substrate isolated LDO for an inductively powered retinal implant to generate a negative substrate voltage of $-2V$ out of a more negative rectified voltage down to $-7V$ is presented. Due to the fact that the negative rectified input voltage is negative relative to substrate, the LDO has to be completely isolated against substrate. The LDO has an Open Loop Gain of $66dB$ and a PSRR of $-81dB$ at low frequencies. The process used is a $350nm$ High Voltage BiCMOS technology.*

Keywords: *Isolated LDO, substrate generation, SoC, inductively powered, biomedical implant*

Introduction

Almost in all types of biomedical implants like retinal implants or pacemakers, supplying power to the electronic device is a challenge. Powering the implants is possible by using batteries or percutaneous lead wires. These require additional surgical operations for battery exchange or pose the risk of infection.

To avoid these drawbacks many biomedical implants are powered inductively through the skin [1]. Power regulation is necessary due to coupling variations. The on-chip supply voltages have to be generated out of the rectified voltages with voltage regulators like Low Drop Out (LDO) regulators [2]. The drawback of state of the art LDOs is that the substrate has to be at the lowest potential on the ASIC [3].

The proposed isolated LDO generates the negative substrate voltage V_{SS} (-2V). Figure 1 shows the architecture of the system. The inductively generated HF is rectified with two half wave rectifiers into a positive and negative rectified voltage. External capacitors are needed to buffer high current pulses. The band gap circuit (BG) generates the reference voltage Vref for the two error amplifiers and is supplied by the positive rectified voltage. The output of both LDOs are fed back to the error amplifiers. As the positive LDO that generates V_{DD} $(+2V)$ is state of the art it will not be further investigated.

The isolated negative LDO generates the negative substrate potential of $-2V$. That means it has to be stable to substrate potential variations. Additionally the input of the LDO is more negative with respect to substrate and has to be completely isolated from substrate.

To our knowledge no other LDO working below the substrate voltage potential exists in open literature.

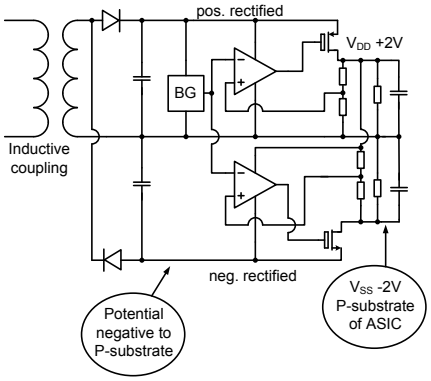

Figure 1: system architecture

Methods

The isolated LDO proposed in this work (Figure 2) has a rectified input voltage that is more negative than the substrate and has to generate the substrate voltage on the output. Because of this negative input voltage against substrate there has to be an isolation from the substrate.

Input voltage to substrate isolation

No PN-junction between negative input and p-substrate is allowed to conduct. Therefore isolated NMOS transistors ("MNiso1" to "MNiso4", Figure 2) have to be used. In the used technology High Voltage (HV) transistors with working ranges up to $50V$ are available. But these so called HV isolated NMOS transistors are not completely isolated (Figure 3). Only the source is isolated by an N-well that has the potential of the drain and therewith the drain has to be positive against the p-substrate.

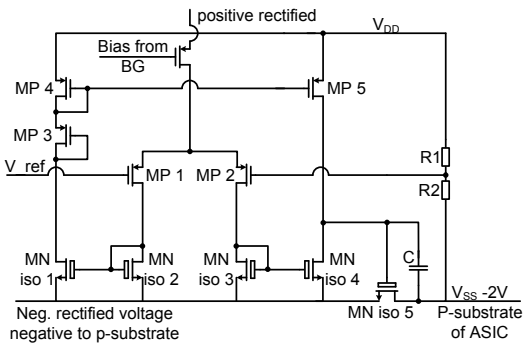

Figure 2: Schematic of isolated negative LDO

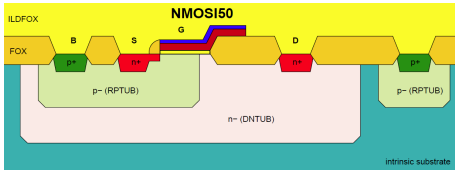

Figure 3: Isolated 50V NMOS transistor with non isolated drain to substrate [4]

Table 1: Specification of isolated negative LDO

	Label	Voltage range
Bias supply	Pos. rect. voltage	0 to +10V
Output driver	V_{DD}	0 to +2V
LDO input	Neg. rect. voltage	0 to -7V
LDO output	V_{SS}: substrate voltage	0 to -2V

The available Low Voltage (LV) transistors are completely isolated. Both source and drain are entirely in a separate N-well. This N-well is in this case connected to a potential of 0V to have non-conducting PN-junctions. Inside this N-well the completely isolated LV-NMOS has its own P-well. This leads to a PNP structure with the N-well at 0V. The substrate to N-well diode and the negative-rectified voltage to N-well diode must not conduct.
As the breakthrough voltage of the diode built by the P-well of the NMOS and the isolating N-well is only $7V$ the negative rectified input voltage must never be below $-7V$. This is guaranteed by a separate HF power regulation circuit in front of the rectifier. This is not discussed here.
The diode connected transistor "MP3" (Figure 2) is used to decrease the drain potential of "MNiso1" to be in safe operation area. Voltage levels can be seen in table 1.

Isolated LDO topology

The isolated negative LDO (Figure 2) consists of an amplifier to compare the reference voltage from the band gap with the feedback resistively divided voltage. This differential PMOS input pair is biased with a current mirrored from the BG supply path.
The load of the differential pair is a current mirror topology to mirror the current with this second stage to the gate of the NMOS transistor "MNiso5" that conducts the maximum load current. This transistor has to be a HV transistor because the gate-source-voltage exceeds the breakdown limit for the low voltage transistors. The use of a half isolated HV transistor is possible because the drain is connected to the substrate and is therefore never below the substrate.

Results

The circuit has been fabricated using a $350nm$ High Voltage BiCMOS technology. The isolated negative LDO has an Open Loop Gain of $66dB$ and a Phase Margin of $92°$ at $2,2MHz$. The Power Supply Rejection Ratio (PSRR) of the negative LDO is $-81dB$ at low frequencies (Figure 4).
Measurement results of the startup of the positive and the negative LDOs are shown in Figure 5. It can be seen that

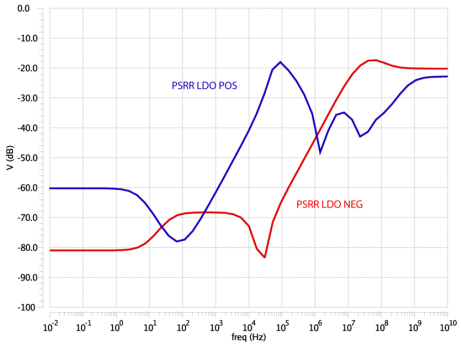

Figure 4: PSRR of LDOs

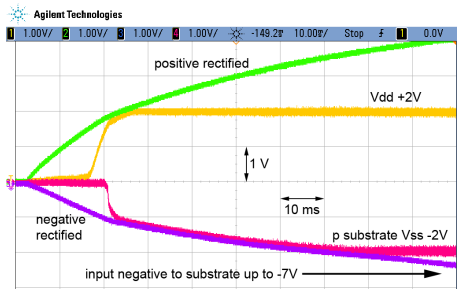

Figure 5: Startup of BG, positive and negative LDO. Negative input can decrease down to -7V.

first the positive LDO has to generate V_{DD} before the negative LDO can generate the negative V_{SS} of $-2V$. This is due to the resistively divided feedback from V_{DD} - V_{SS} to the error amplifier input of the negative LDO. Measurements show that the input voltage can be negative down to $-7V$ and no PN-junction is conducting.

Discussion

An isolated LDO with negative input referred to substrate to generate the substrate potential of $-2V$ has been presented. The LDO is produced and measured using a $350nm$ High Voltage BiCMOS technology. Measurements show that the LDO input is completely isolated against substrate.

Bibliography

[1] A. Rothermel, L. Liu, N. Aryan, M. Fischer, J. Wuenschmann, S. Kibbel, and A. Harscher, “A cmos chip with active pixel array and specific test features for subretinal implantation,” *Solid-State Circuits, IEEE Journal of*, vol. 44, pp. 290 –300, jan. 2009.

[2] G. Rincon-Mora and P. Allen, “A low-voltage, low quiescent current, low drop-out regulator,” *Solid-State Circuits, IEEE Journal of*, vol. 33, no. 1, pp. 36–44, 1998.

[3] Linear Technology, *LT3032 Series - Dual 150mA Positive/Negative Low Noise Low Dropout Linear Regulator*.

[4] M. Schrems, “The role of ic technologies in supporting low cost electromobility,” *Auto.E-Motion. URL:http://www.ams.com/autoemotion*, 2011.